Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, APRIL / MAY 2019

SUBJECT: ANALOG SYSTEM DESIGN [ELE 2204]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 04 May 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Determine the input impedance and output voltage for the circuit shown in fig 1A. (02)

1B For the ideal Op amp circuit shown in fig 1B. Find v_0 and i_x, if $i_s = 8A$. (03)

1C A certain instrumentation amplifier has a gain of 40dB and a common-mode rejection ratio of 100dB. It is used in noisy environment in which the signal has a level of 50mV, and the common-mode noise level is 100mV. Determine (a) common-mode gain (b) signal output (c) noise output and (d) output signal voltage to noise voltage ratio. (03)

1D Define Slew Rate. What is the significance of slew rate in Op amp applications. (02)

2A For the circuit shown in fig 2A, (a) plot the magnitude response $M(\omega)$ (b) determine the phase shift and time delay at 1KHz. (03)

2B. Design a practical integrator with $f_a = 5KHz$. Assume $C = 10nF$ if required. Draw the circuit diagram. (03)

2C. Draw the transfer characteristics for the precision rectifier shown in fig 2C. Assume ideal Op amp and practical diode and input $V_i = 10 \sin \omega t$. (04)

3A Using just one op-amp powered from ± 12V regulated supplies, design a circuit to yield Vo = 3 – 2.5V1 – 5V2 where V1 and V2 are input signals. Assume feedback resistance of 10 kΩ, if required. (03)

3B Design an Op-amp based circuit which generates a triangular wave of frequency 5kHz and 5V peak. Assume saturation voltage of ±10V and capacitor of 0.1μF if required. (03)

3C. Using the pole-zero concept, design a 4th order Butterworth high pass filter with a cut-off frequency of 8kHz. Assume capacitor of 0.1μF if required. Determine the overall gain of filter. (04)

4A Using 555 timers design a circuit to generate the waveform shown in Fig 4A. Assume C=0.047uF if required. Generate V02 using V01. (04)

4B Draw the circuit diagram and explain the working of opamp based positive peak detector. (02)

4C Realize a circuit to implement a VTC as shown in Fig 4C. Assume Vsat=±12V, Input is 10sinwt. Draw the input and output waveforms with transition points. Assume feedback resistance of 10 kΩ, if required. (04)

5A Derive expressions for input and output resistance of an Amplifier which makes use of Voltage shunt feedback topology. Also draw the MOSFET based circuit which incorporates this feedback. (05)

5B What is Desensitivity factor? State the significance of D in Feedback Amplifiers (02)

5C For the circuit of fig 5C, determine the (a) feedback voltage (b) frequency of the output waveform $v_0(t)$. Assume $\pm V_{sat} = \pm 12V$. (03)

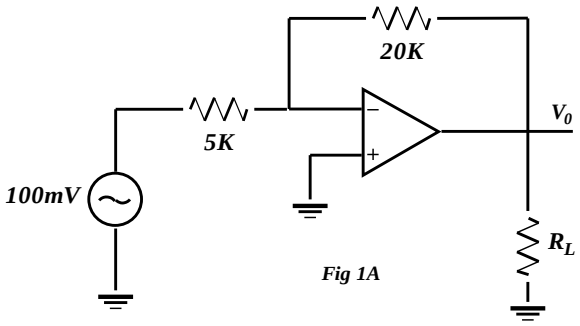

Fig 1A

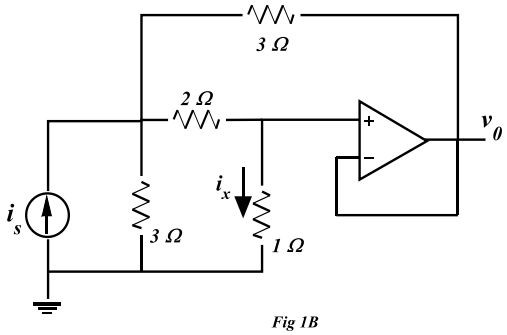

Fig 1B

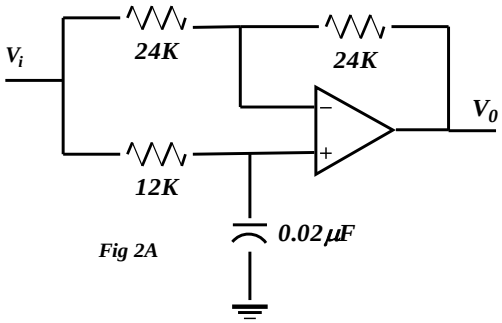

Fig 2A

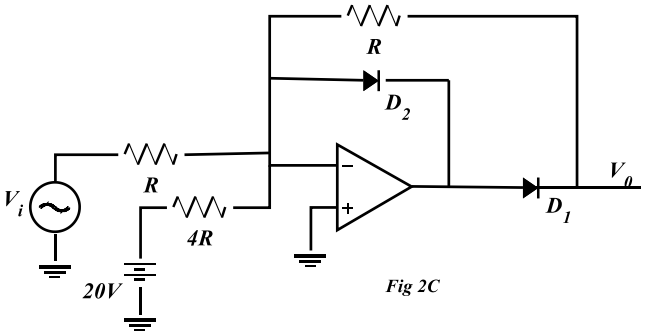

Fig 2C

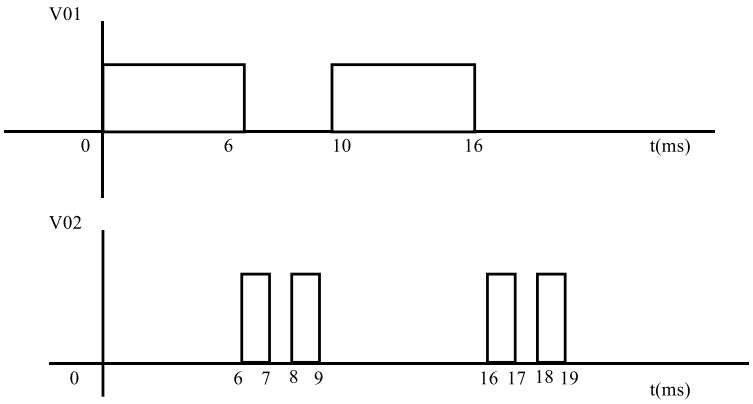

Fig 4A

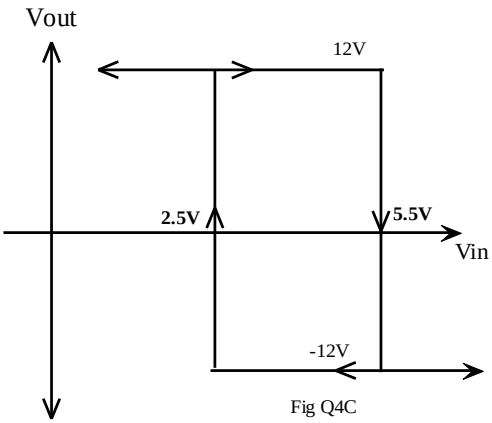

Fig Q4C

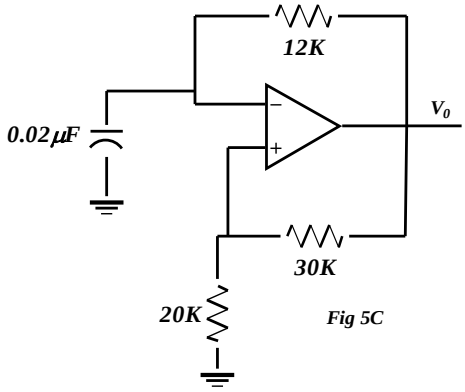

Fig 5C