Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent Institution of MAHE, Manipal)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKEUP EXAMINATIONS, JUNE 2019
DIGITAL SYSTEM DESIGN AND COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date:17 June 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Explain the steps in Silicon processing. ***(03)***

1B. Write a behavioral Verilog code for BCD adder and display the BCD sum on the seven segment display. ***(03)***

1C. Write a Verilog code for JK flip flop. Using this flip fop as an instance, Write a structural Verilog code for a 3 bit UP counter. ***(04)***

2A. A digital system has one input x and one output z .The output Z=1 occurs every time the input sequence 1010 and 011 is detected. Draw the state diagram for the sequence detector using mealy machine and write the Verilog HDL code for it. ***(04)***

2B. A digital circuit includes a light sensor with a digital output, dark, that is true (high voltage) when there is no ambient light, or false (low voltage) otherwise. The circuit also includes a switch that determines whether the digital signal lamp_enabled is low or high (that is, false or true, respectively). Thus, in the circuit, the signal lamp_lit is true if lamp_enabled is true *and* dark is true, and is false otherwise. Use gate level model Verilog HDL to realize the digital circuit for a night-light that is only lit when the switch is on and the light sensor shows that it is dark. ***(03)***

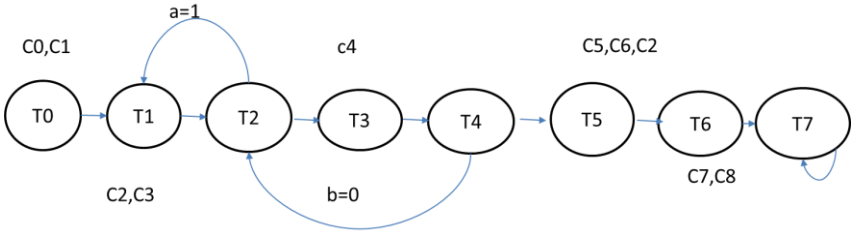
2C. Develop the Verilog HDL code for 4 bit universal shift register. ***(03)***

3A. Draw the architecture of a stack based machine and explain the functions of the components involved in them. ***(04)***

3B. Perform 13 X 20 using Add and Shift method. ***(04)***

3C. Differentiate between RISC and CISC. ***(02)***

4A. For the state diagram shown below



i) Draw Micro programmed Control Unit.
ii) Write the Micro program.
iii) Determine the Size of Control Memory. ***(04)***

4B. For the same question 4A. Calculate % Saving made for the following
i)Using Decoders only
ii)By elimination of branch address ***(04)***

4C. With neat Diagram explain Daisy chain Method of servicing multiple Interrupts. ***(02)***

5A. Calculate the average access time, ratio of main memory to cache memory access time and efficiency of the memory system whose parameter includes below.
Cache access time =100ns , Main Memory access time =350ns, and hit ratio =0.7 ***(03)***

5B. Assume a main memory has 4 page frame and initially all pages are empty. Consider following streams of page requests 1,2,3,4,5,1,2,6,1,2,3,4,5,6,5 . Determine the hit ratio for FIFO and LRU replacement policy. ***(03)***

5C. With flow chart, Write note on FPGA Design flow. ***(04)***