Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, APRIL / MAY 2019

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 02, May 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. With the help of four bit ripple carry adder block diagram, explain the top down and bottom up digital design methodologies. ***(03)***

1B. Write a Verilog HDL code for a one bit magnitude comparator using dataflow modeling. ***(03)***

1C. Alissa arrives home, but her keypad lock has been rewired and the old code no longer works. A piece of paper taped to it showing the equation of the FSM based door locking circuit implemented with D flip flops. The equations of the FSM are :

z (keypad lock) = Q_1Q_2,

D1 = $Q_1.\overline{Q_2}\,x + \overline{Q_1}\,Q_2\bar{x}$, D2= x

Where D1 and D2 are the flip flop inputs, x is the external input, z is the external output, Q_1 and Q_2 are the flip flop states. Draw the state diagram of the circuit and develop a Verilog HDL code for the state diagram using behavioral modeling. ***(04)***

2A. Construct a ring counter (sequence 1000 – 0100 -0010 -0001) using structural modeling. Use 2 bit up counter and 2 to 4 decoder as the instances for the ring counter. ***(03)***

2B. Develop the Verilog HDL code for a 3 bit even parity generator using gate level modeling. ***(03)***

2C. Write functions for addition, subtraction, multiplication and division. Using these functions write a Verilog HDL code for the arithmetic circuit which performs the operation according to the given table. A and B are one bit input. Use procedural assignment statement for the function call.

Select input	Operation
00	A+B
01	A-B
10	AX B
11	A÷B

(04)

3A. Given an instruction set and the corresponding relative frequency, encode using Huffman's method and calculate the redundancy. Also calculate the redundancy if block code encoding technique is used.

Instruction	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8
Relative frequency	0.11	0.31	0.25	0.04	0.04	0.01	0.05	0.14	0.05

(04)

3B. Perform **18 X -25** using Modified Booth's algorithm. ***(04)***

3C. Identify the addressing modes and justify the same, for the following instructions.

i) HLT

ii) MOV @#6000, R5 ***(02)***

4A. Perform the following for 4 bit Add and Shift multiplication algorithm

i) Write a register transfer logic and develop the control signals

ii) Draw the flow chart

iii) Design the controller using Hardwired approach ***(05)***

4B. Prove that Nano memory saves the space of control memory size with an example. ***(03)***

4C. List out the differences between two Priority interrupt handling techniques. ***(02)***

5A. The Parameter of Computer Memory System are specified as follows

Main Memory Size = 4096 blocks

Cache Memory Size =1024 blocks

Block Size =16 words

Determine the Size of the tag field of Main memory address under the following conditions

i) Fully associative Mapping

ii) Direct Mapping

iii) Set associative mapping with 8 block /set ***(03)***

5B. Write the differences between Paging and Segmentation. ***(03)***

5C. List the CPLD/ FPGA programming technologies. Explain any two with the neat diagram. ***(04)***