Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (DEC / ME) DEGREE END SEMESTER XAMINATION
JUNE 2019
SUBJECT: CAD TOOLS FOR VLSI DESIGN (ECE - 5234)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Apply Hu algorithm for the given data flow graph shown in **Fig. 1A**. Assume γ=4, P(0)=1, P(1)=3, P(2)=4, P(3)=2, P(4)=2. Determine the resource constraints. Draw the scheduled graph with resource constraints.

1B. Determine the prime implicants for the following function using iterated consensus method $F=\sum m(0, 2, 3, 4, 5, 6)$.

1C. Explain ASIC design flow.

(5+3+2)

2A. Draw ROBDD for 3-bit up/down counter. Show all the steps. Also perform If-Then-Else(ITE) algorithm for the same.

2B. Explain LIST-L scheduling algorithm with an example.

2C. Explain the steps for High level synthesis.

(5+3+2)

3A. Find the essential prime implicant for the set of prime implicants $F=\{C_1, C_2, C_3\}$ where $C_1=x_1'x_3'x_4'$ $C_2=x_1x_2$ $C_3=x_3x_4$ using ESPRESSO algorithm.

3B. Determine the test vector for the sequential circuit shown in **Fig. 3B** using ITG.

3C. Define latency, mobility and resource constraints.

(5+3+2)

4A. Implement the given function using ACT3 S module. Find the number of logic modules required to implement. $D1=X'+Y_1$, $D2=XY_2' + X'Y_1'$, $Z=XY_1$

4B. Apply clique partitioning algorithm for the sequencing graph shown in **Fig. 1A**. Determine the operation binding resources for MUL and ALU. Show all the steps.

4C. Perform ITE for the function F=ab+cd in the order of a-c-b-d.

(5+3+2)

5A. Using tabular method, obtain prime implicants and minimal expression for the following function: $F=\sum m(6, 7, 8, 9)+d(10, 11, 12, 13, 14, 15)$

5B. Find the sequence for the faulty and fault free circuit using signature analysis technique to test the single stuck at faults (α at SA_0, β at SA_1) shown in **Fig. 5B**. Assume it's a 4-bit shift register and the third bit from MSB is connected as feedback to the one input of XOR gate.

5C. Explain Y chart. (5+3+2)

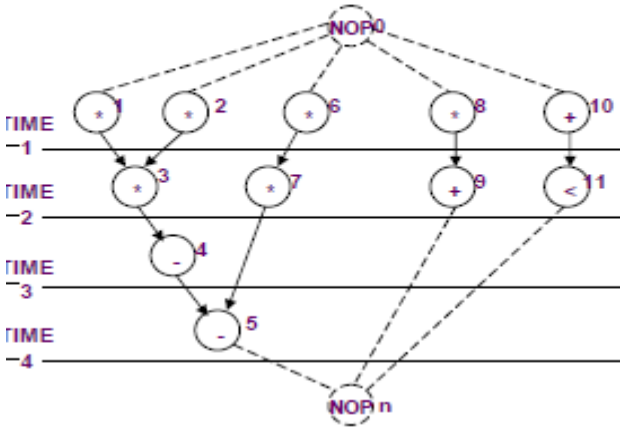

Fig. 1A

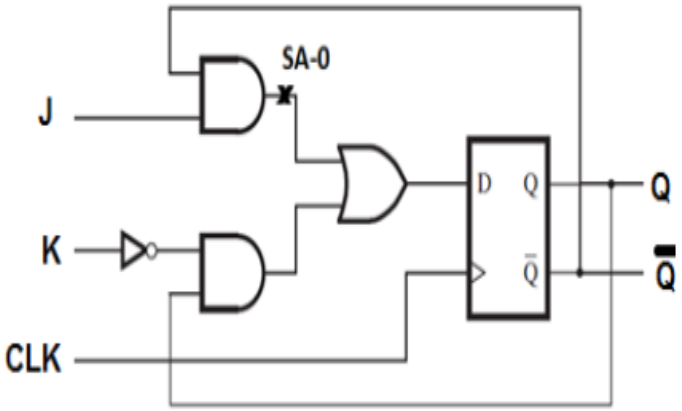

Fig. 3B

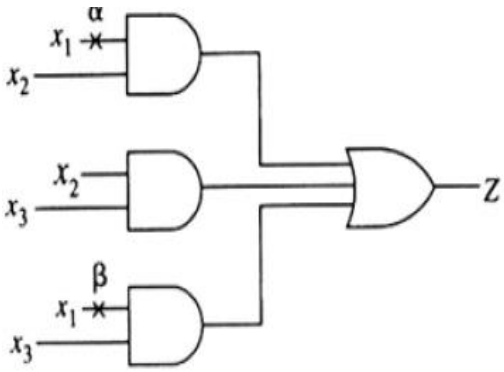

Fig. 5B