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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*(A constituent unit of MAHE, Manipal)*

**SECOND SEMESTER M. TECH. (DEC/ME) DEGREE END SEMESTER EXAMINATION**
**JUNE 2019**
**SUBJECT: VLSI PHYSICAL DESIGN AND VERIFICATION (ECE - 5258)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**

- Answer ALL the questions.
- Missing data may be suitably assumed.

1A. Derive an expression using exact Zero Skew Algorithm (ZSA) for the given **Figure 1A** ($\pi$ model of RC network is used here) to get the tapping point position (indicate in figure) for the cases x = 0, x < 1 and x > 1. Here T1, T2 are two sub trees and t1, t2 are the delay between the nodes and leaves, $\alpha$ is the resistance per unit length and $\beta$ is the capacitance per unit length.

1B. An application of PROM is to realize LUTs for arithmetic functions. Using a PROM of the smallest appropriate size, draw the logic diagram in PLD notations for a PROM realization of the LUT correspond to the decimal arithmetic expression $F(X) = X + 2$ for $0 \leq X \leq 7$, where F(X) and X are expressed in binary.

(6+4)

2A. For the logic circuit given in **Figure 2A**, draw the (a) timing graph, determine the (b) Actual arrival time (AAT), (c) Required arrival time (RAT), (d) slack of each node and (e) highlight the critical path. The AATs of the inputs are in angular brackets, the delays are in parentheses, and the RAT of the output is in square brackets.

2B. Write the pseudo code for unconstrained Left Edge Algorithm (LEA).

2C. Explain the following terms, design verification, validation and testing?

(5+3+2)

3A. Estimate the total wire length for a five-pin net shown in **Figure 3A** with pins a, b, c, d and e. Draw a rectilinear minimum-length chain, a rectilinear minimum spanning tree (RMST), and a rectilinear Steiner minimum tree (RSMT) to connect all pins and also calculate the weighted total wire length using each estimation technique respectively. Assume each grid edge has unit length and weight=2.

3B. Briefly explain the simulation based verification methodology with block diagram?

3C. Briefly explain the clock tree synthesis and write the pseudo code for the method of means and medians (MMM).

(4+3+3)

4A. Briefly explain all the steps in power and ground routing using “mesh topology” with neat diagram.

4B. What is die yield? Assume a wafer size of 12 inch, a die size of 2.5 $cm^2$, 1 defects/$cm^2$, and $\alpha$ is parameter=3 (equal to number of masks). Determine the die yield of this CMOS process technology.

4C. Find the critical path in the half adder which is made of 2 i/p XOR, 2 i/p AND and 2i/p OR gate. Check through path sensitization whether it is a true or false path (Assume no wire delay). The intrinsic delay of XOR, AND and OR gate is 6, 4, 4 units respectively.

(4+3+3)

5A. For a given netlist of five cells [a, b, c, d, e] and six nets N1={a, e}, N2={a, b}, N3={a, c, d}, N4={a, d}, N5={b, c, d}, N6={b, d}, apply Linear Ordering Algorithm (LOA). Consider 'a' as seed block.

5B. What are the major components of a simulator? Briefly explain event driven simulator and how the timing wheel mange them? What are the five layers of events and their order of execution taken in Verilog IEEE standards?

(5+5)

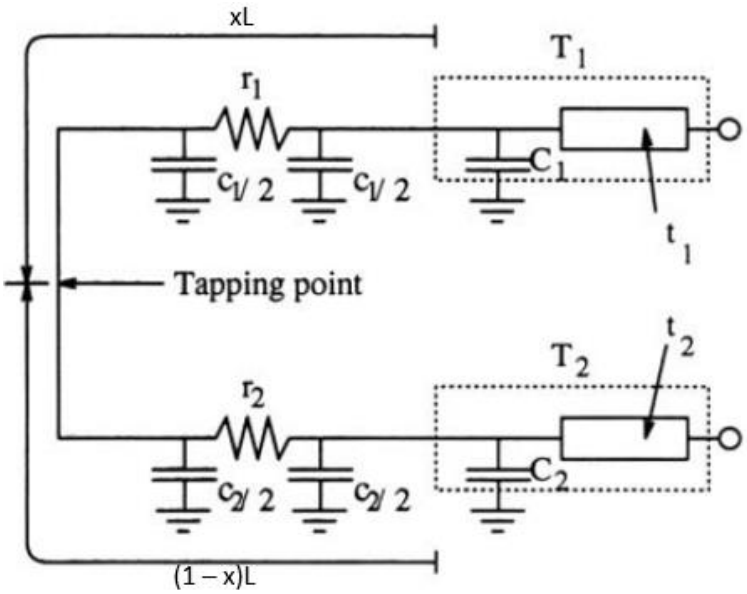


**Figure 1A**

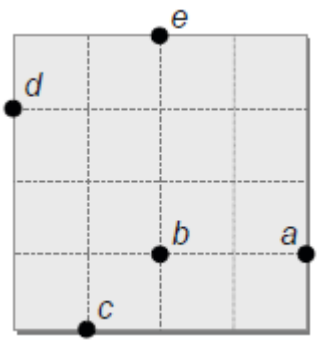


**Figure 3A**

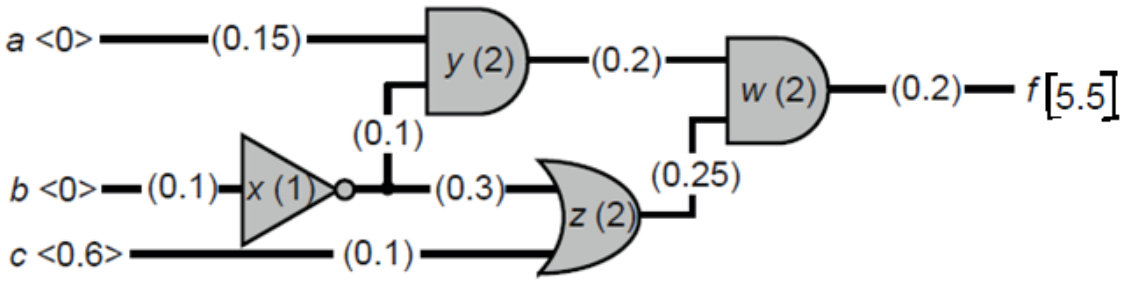


**Figure 2A**