Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (DEC/ME) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2019
SUBJECT: CAD TOOLS FOR VLSI DESIGN (ECE - 5234)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the sequencing graph for the given function:
F= [(C+(A*B))-((B*C)+A)]<[P+Q]+Y. Assume all the operations are having unit execution delay. Calculate latency using ASAP and mobility using ALAP algorithm.

1B. Determine the prime implicant for the following function using iterated consensus method
F(A,B,C) = A'B'C'+A'BC'+A'BC+AB'C'+AB'C+ ABC'

1C. Draw control and data flow graph for the following sequential statements:
X=A*B, Y=C+D, if X<Y then Z=Y-X else Z=X-Y.

(5+3+2)

2A. Draw the sequencing graph for F = [C - (a * b * d) < (a * b * c) + d] * [X + Y]. Apply Clique partitioning algorithm and determine the operation binding resources for MUL and ALU. Show all the steps.

2B. Find the test vector using Iterative test generator for the following expressions: $Y_1^+=X'+Y_1$, $Y_2^+=XY_2'+X'Y_1$, $Z=XY_1$. Z is the output, X is the input Y_1 & Y_2 are the previous states and Y_1^+ & Y_2^+ are the next states of the flipflops. Consider SA_0 fault is at Y_2' at Y_2^+ node.

2C Define the term exact minimization and heuristic minimization with an example each.

(5+3+2)

3A. Find the essential prime implicant for the set of prime implicants F={C_1, C_2, C_3, C_4} where $C_1 = x_1'x_3'x_4'$ $C_2 = x_1x_2$ $C_3 = x_3x_4$ $C_4 = x_2x_3'x_4'$ using ESPRESSO algorithm.

3B. Draw ROBDD for 3 bit synchronous even counter. Show all the steps starting from OBDD. Perform ITE algorithm for ROBDD.

3C. Explain Gajski's Y Chart.

(5+3+2)

4A. Determine minimum latency under resource constraint for the data flow graph shown in **Fig. 4A** using LIST-L scheduling algorithm. Draw the scheduled graph. Assume mobility m1 = m2 = m3 = m4 = m5 = 0, m6 = m7 = 1, m8 = m9 = m10 = m11 = 2.

4B. Implement full adder using 2 half adders and 1 OR gate using ACT3 logic module. Determine the number of logic modules required to implement.

4C. Draw the stick diagram for the function F = (A XOR B)

(5+3+2)

5A. Implement the circuit shown in **Fig. 5A** using ACT-2S module. Determine the number of logic modules required to implement.

5B. Find out the signature for the faulty and fault free circuit for Transparent high latch. Consider 4-bit shift register, one input of the XOR gate is connected as feedback to the second bit from the right. The SA_0 fault is given at D input not to the feedback input.

5C. Write the expression to calculate the lower bound of resources to complete a schedule using Hu algorithm.

(5+3+2)

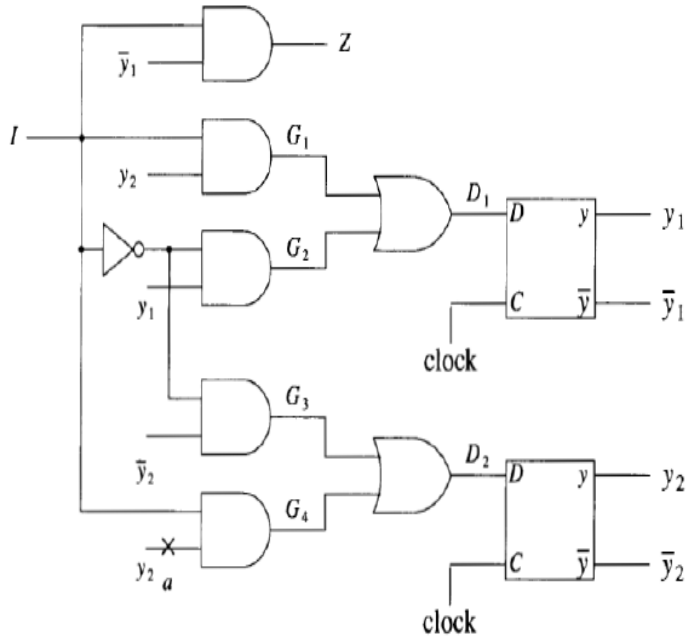

Fig. 5A

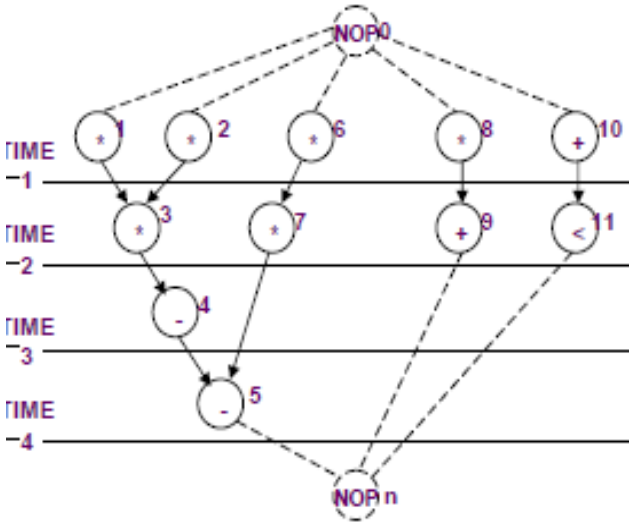

Fig. 4A