Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (ME) DEGREE END SEMESTER EXAMINATION
JUNE 2019
SUBJECT: CMOS MIXED SIGNAL DESIGN (ECE - 5222)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Give OTA-C current-mode Tow-Thomas[TT] biquad circuit and derive expressions for two current-in current-output transfer functions. Give the expression for pole frequency and pole-Q.

1B. Define the following terms:
i) Dynamic range ii) Total Harmonic Distortion (THD) iii) Sensitivity

1C. Derive the transfer function for fully differential OTA-C circuit in **Fig. 1C**. Give your comments.

(5+3+2)

2A. Design a RLC band-pass biquad using active transconductor blocks with a Q of 10 and a cut-off frequency of 1.59MHz. Give comments about sensitivity and tunability.

2B. Show that the switched-capacitor circuits shown in **Fig. 2B** behave like resistors, for $f < f_{clk}$ with the resistor values shown.

2C. Realise the switched capacitor equivalent of the active RC filter structure in **Fig. 2C** and analyse the behaviour.

(5+3+2)

3A. i) State the advantages offered by current-mode signal processing over conventional analog voltage signal processing.
ii) With a schematic circuit explain the working of 4-bit charge scaling DAC.

3B. Give the g_m-C current-mode realisation of RLC parallel resonator circuit shown in **Fig. 3B**. Derive the expressions for different transfer functions. Give your comments.

3C. Demonstrate the advantages of using Deboo integrator in active-RC Tow-Thomas Biquad realization.

(5+3+2)

4A. Derive the expression for all current-mode transfer functions for the circuit in **Fig. 4A**. Are the biquads independently tunable? Give your comments about the filter structure.

4B. Explain the practical OTA macro models.

4C. Give OTA-C implementation of :
i) floating resistor (series element) ii) floating resistor (shunt element)

(5+3+2)

5A. i) Show how Miller's theorem can be used to realize negative capacitance circuit using OTA.
ii) Design a OTA-C voltage-mode first-order all-pass filter for a cut-off frequency of 10MHz.

5B. Explain the single bit sigma-delta ADC structure.

5C. Discuss the analog layout considerations for following:
i) MOS devices in differential amplifier ii) Capacitor array in charge scaling DAC.

(5+3+2)

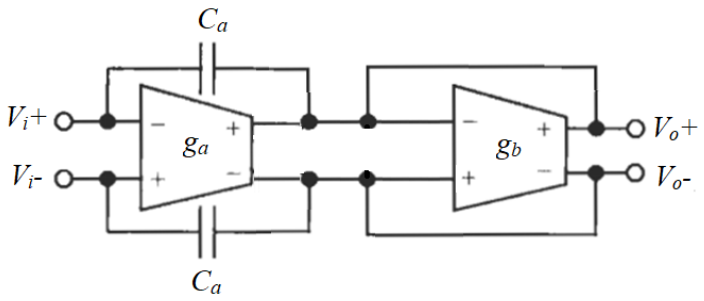

Fig. 1C

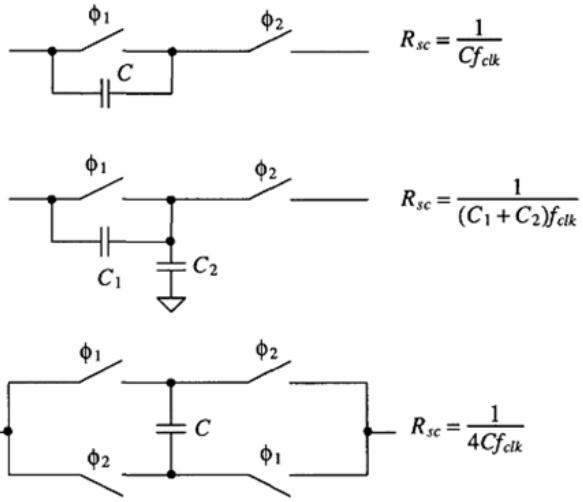

Fig. 2B

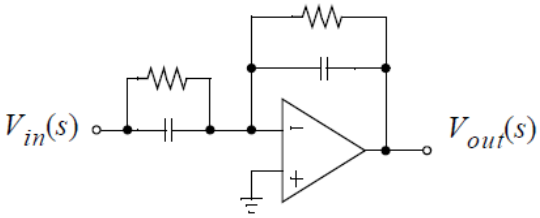

Fig. 2C

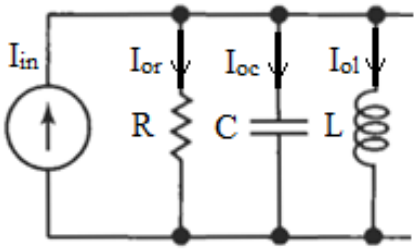

Fig. 3B

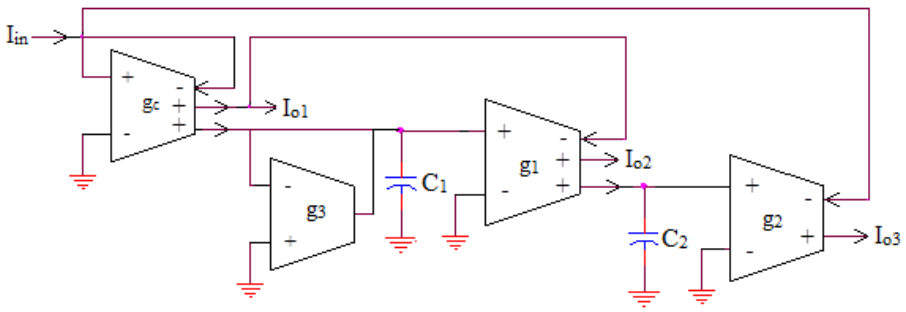

Fig. 4A