Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (ME) DEGREE END SEMESTER EXAMINATION
JUNE 2019
SUBJECT: LOW POWER VLSI DESIGN (ECE - 5221)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss and distinguish power aware and low power design approaches with suitable examples.

1B. Derive the expression for short circuit power in CMOS and highlight the significance of the expression.

1C. Explain the problems encountered when we use level converters in the CMOS circuit design.

(4+3+3)

2A. Explain the concept of bus segmentation employed to reduce dynamic power with suitable illustration.

2B. With the help of a neat diagram, explain bus invert coding. What are its salient features ? discuss.

2C. Explain the motivation for low swing buses in VLSI circuits highlighting it's merits and demerits.

(4+3+3)

3A. List and explain any TWO techniques used to reduce the subthreshold leakage.

3B. Discuss the impact of crosstalk and techniques employed to reduce crosstalk in interconnects.

(5+5)

4A. Explain i) Power gating and ii) Clock gating for low power. Also show how it can be implemented using HDL code.

4B. Explain implementation of low swing busses for power reduction in VLSI circuits highlighting it's merits and demerits.

4C. Assume that the Boolean function F = (AB+CD) is design using AOI. If the probabilities of the inputs A and B are 0.6 each and that of C and D are 0.4 respectively. Estimate the switching activity at the output.

(4+3+3)

5A. With the help of examples, explain any THREE techniques employed in coding/software for achieving Low Power.

5B. Discuss the functions performed by ACPI and Explain the role of ACPI in mower management at the system level.

(5+5)