Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (DEC & ME) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2019
SUBJECT: VLSI TESTING AND TESTABILITY (ECE -5259)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. A three input gate LEMON (**Fig. 1A (i)**), who's characteristic are shown in **Fig. 1A (ii)**, has been mass-produced by an unfortunate Chinese company. Experimental evidence shows that input combination shown below in **Fig. 1A (iii)** are responsible to BOMB to explode. The company official has hired "**Sherlock Homes"** to find the cause of it. Sherlock Homes has following tasks to do:
(i) to find the possible combinations for which BOMB will exploded.
(ii) to check whether the circuit is completely useless?
(iii) to look whether fault/faults can be identifiable? Use any fault detection technique.

1B. Find the T.V using FAN algorithm for SA1 as shown in **Fig. 1B**.

1C. Find the T.V using SOCRATES algorithm for SA1 as shown in **Fig. 1B**.

(4+3+3)

2A. Find the Test vector of sequential circuit using Time Frame expansion method for the circuit shown in **Fig. 2A.**

2B. Consider the circuit shown in **Fig. 2B** with 'a' is at SA1 and 'b' is at SA0. **Use Boolean difference technique** to find (i) Z, Z_a and Z_b. (ii) check if (101) detects Z_a (iii) check if (101) distinguishes Z_a & Z_b.

2C. Explain the Transition delay fault simulation with example.

(4+3+3)

3A. Consider the circuit shown in **Fig. 3A**. Find the test vector using PODEM algorithm.

3B. Apply SCOAP to **Fig. 3B**.

3C. Apply Fault equivalence and Fault dominance rule for the circuit shown in **Fig. 3C**.

(4+3+3)

4A. Consider the BIST system shown in **Fig. 4A**. Find which fault are detected B SA1, C SA0 and C SA1? Initial content of Pattern generator is 001 and Response compactor is 000.

4B. Consider the Function, F(a ,b, c)= a' b' c' + a' b c' + a b c' with SA0 at input a. Fill the Table in the following format.

Output (X) for R Spectra	Output (Y) for S Spectra	R Spectra Coefficient	S Spectra Coefficient	Faulty R Spectra Coefficient

4C. **TSMC** is going to ship one billion ICs in 2015. In the testing lab, a testing engineer have found that Defect level should be within 250 defects per million in order to have maximum fault coverage. For this Yield and Fault coverage statistics has to be enumerated, **Table 4C**. Populate the **Table 4C**.

Table 4C

Yield (Y,%)	10	50	90	95	99
Fault coverage, (FC,%)					

(4+3+3)

5A. Consider the function, F= ab + a' c + b' c'. Determine the read muller expansions and draw the corresponding circuit.

5B. (i) Imagine a three-dimensional VLSI system in the form of a cube, where the volume contains transistors and interconnects, and pins are placed on the surface. We assume that the problems of power dissipation and cooling have been worked out to make such a device possible. Derive Rent's rule for this device. Is the test problem for the cube more, or less, complex than that for the flat chip?

(ii) Can we test this circuit shown in **Fig. 5B(ii)**

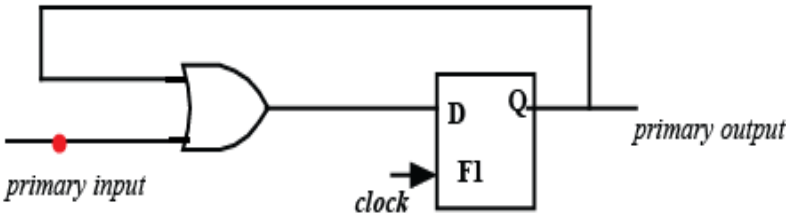

Fig. 5B (ii)

5C. Explain the set-up for A/D converter test. Briefly explain about each block.

(4+3+3)

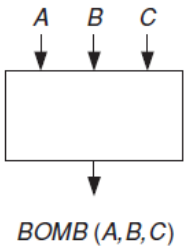

Fig. 1A(i)

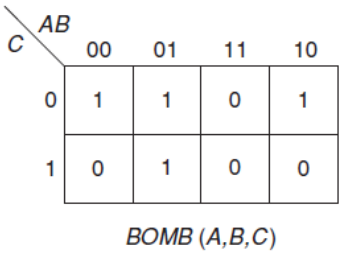

Fig. 1A (ii) Correct Combination

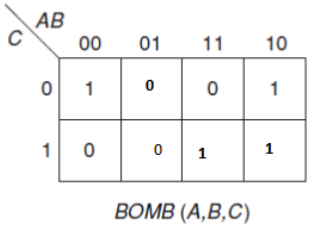

Fig. 1A (iii) Wrong Combination

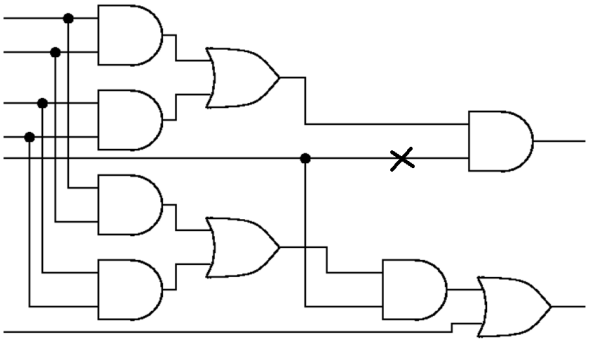

Fig. 1B

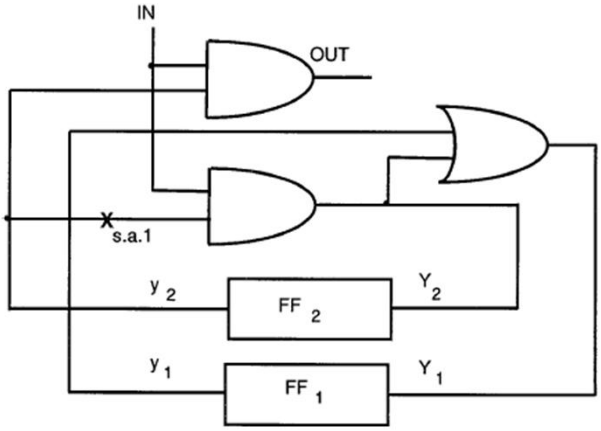

Fig. 2A

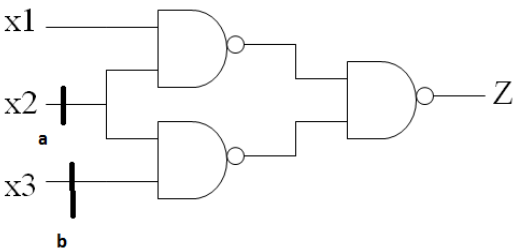

Fig. 2B

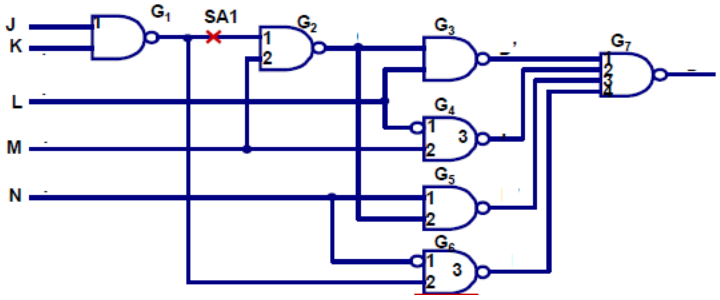

Fig. 3A

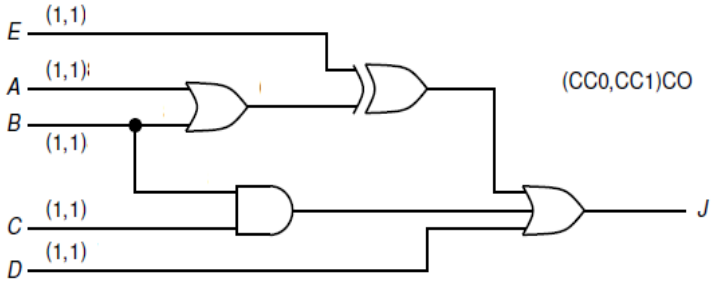

Fig. 3B

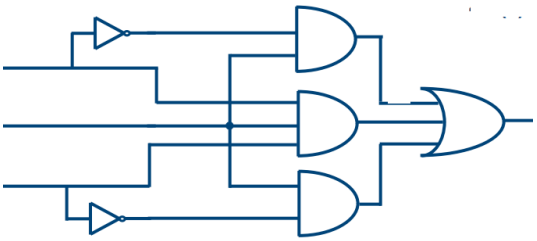

Fig. 3C

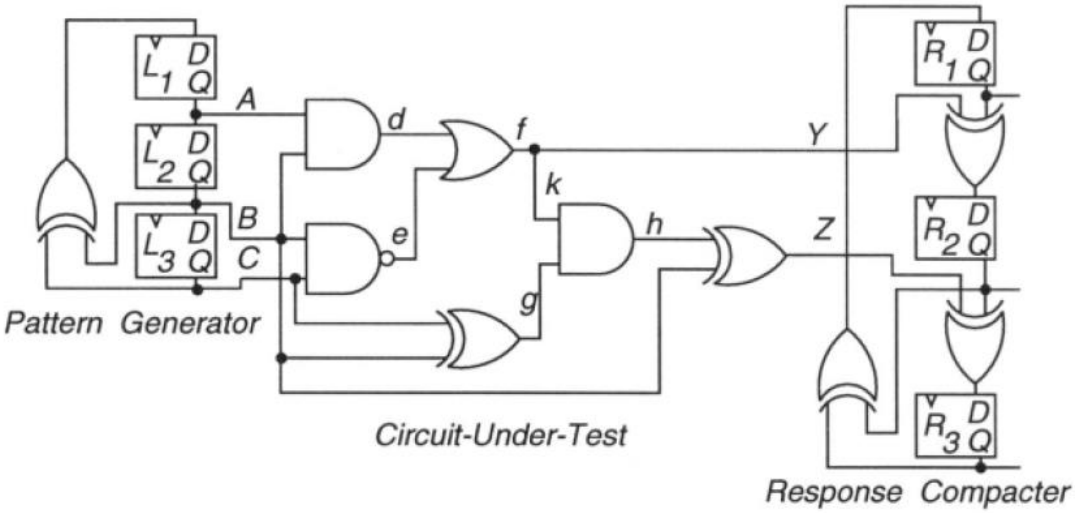

Fig. 4A