Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M. TECH. (ME) DEGREE END SEMESTER EXAMINATION
APRIL/MAY-2019
SUBJECT: VLSI PHYSICAL DESIGN AND VERIFICATION (ECE - 5258)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer ALL the questions.
- Missing data may be suitably assumed.

1A. Calculate the delay for the given Figure 1A, using CPM. Assume each block is an inverting logic gate and all the primary inputs have arrival times of 0 units for both rise and fall delay. By considering the required arrival time for rise and fall transition is of 10 units, calculate the worst case arrival time, required time, slack and identify the critical path.

1B. Write the Xilinx Integrated Software Environmental (ISE) tool development flow with block diagram and represent the input, output files in each stage.

(5+5)

2A. Briefly explain the electromigration effect and criteria for electro migration failure in supply rails. A device has a required lifetime of 10 years. Measurements for AI electromigration using an accelerated testing method indicates that A (an empirical fitting coefficient) = 2×10^7 hr-cm^2/ampere and $\Delta H = 0.85$ eV. What is the maximum allowable current density in AI interconnect at 125^0C? Verify if $J_{avg} = 10^7$ Amp/Cm^2, will it cause electromigration failure or not.

2B. Sketch a 2-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter. Compute the best and worst case rising and falling propagation delays of the NOR gate driving *h* identical NOR gates using the Elmore delay model.

2C. Compare H tree clock network with X tree clock network.

(5+3+2)

3A. For the given polish expression PE = 435H1V67VH2V8HV, answer the followings:

(a) Does the above expression have the balloting property? Justify your answer.

(b) Is the above expression is a normalized Polish expression? Justify your answer.

(c) Why is it desirable to restrict ourselves to only normalized Polish expression?

(d) Give the slicing tree corresponding to the Polish expression PE?

(e) Assume that (width, height) of the modules 1 through 8 are {(5, 3), (2, 3), (6, 3), (2, 5), (6, 2), (5, 1), (3, 8), (6, 3)}. What is the minimum area of the slicing floorplan? Rotation is not allowed.

Draw the floorplan and place the lower left corner of each block to the lower left corner of its room.

3B. For the given channel routing problem as shown in Figure 3B, find S (col), where col = a, b, c, d, e, f, g, and draw the Vertical Constraint graph, Horizontal Constraint Graphs of nets A, B, C, D, E and F.

(6+4)

4A. What is Binary Decision Diagram (BDD) and how it is useful in verification? For the BDD in Figure 4A, do the following:

a. Is the BDD reduced one?

b. Derive the function represented by the BDD in sum-of-products form. Repeat (b) for product of sums.

4B. Briefly explain all the steps with neat diagrams used in concentric circle method for pin assignment between a block and all its related pins in other blocks.

4C. Mention the need and objectives of circuit partitioning in VLSI.

(5+3+2)

5A. Discuss the need and advantages of cycle based simulators over event driven simulators. Do the levelization and apply the topological sort using Depth First Search (DFS) algorithm for the unit delay circuit shown in Figure 5A to get the proper evaluation order for steady state simulation (Assume no wire delay).

5B. Briefly explain formal verification method using the block diagram.

5C. Find the minimum clock period of the circuit shown in Figure 5C.

(5+3+2)

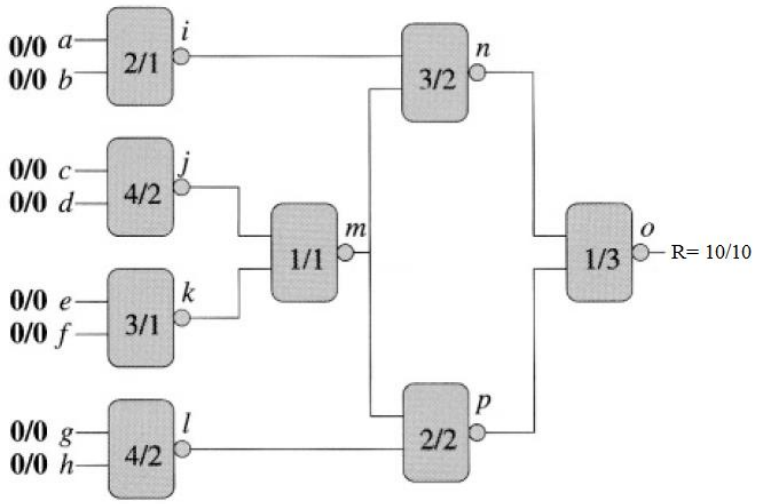

Figure 1A

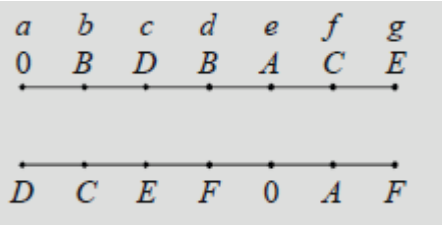

Figure 3B

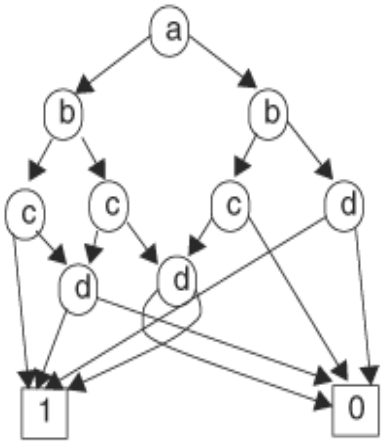

Figure 4A

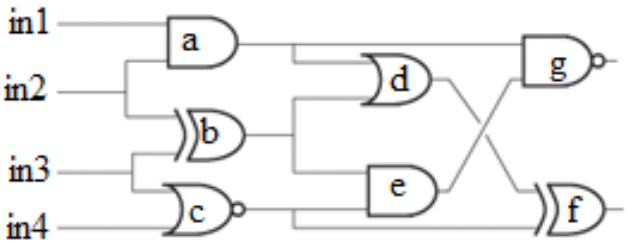

Figure 5A

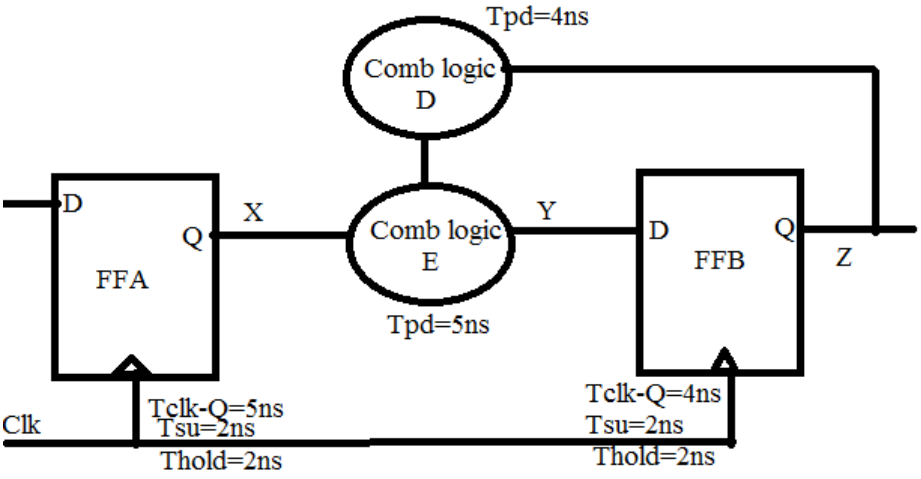

Figure 5C