Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.TECH. (DEC/ME) DEGREE END SEMESTER EXAMINATION
JUNE 2019
SUBJECT: VLSI TESTING AND TESTABILITY (ECE - 5259)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain the testing Process with neat diagram.

1B. Find singular cover and propagating D cube for the circuit shown in **Figure 1B.**

1C. For the circuit shown in **Figure 1C**, find the Test vector for G_1 at SA1 using Boolean difference properties only. Specify the properties used in each step of solutions.

(4+3+3)

2A. Consider the function, F(a,b,c)= 102+ 110+200. Find the T.V using Fault Table method for a and c at SA0 and SA1 respectively.

2B. Apply path sensitization technique to circuit of figure 2B with output of Gate 2 at SA0.

2C. The test vector (A, B, C, D, E, F, G, H) = (0, 1, 1, 1, 1, 1, 1, 1) was applied to the circuit shown in **Figure 3C** and output f indicated an error. What are the single stuck-at faults in this network that could cause the output to be erroneous?

(4+3+3)

3A. Generate a TEST using ATPG for the fault A at SA1 shown in Figure 3A by filling the Table. While you are performing the unknown algorithm, follow the rules given below.
Order: Try to excite the fault first then propagate.
- *Backtrace: Follow a path from the objective to a primary input while always following the alphabetical order (e.g. if a gate has input A and B, backtrace on that gate goes to line A first.*
- *PI assignment: Always assign 0 first, then assign 1 in case of backtrack.*
- *Choice of D or D_bar : Always try to propagate a D or D_bar from the D-frontier which has the shortest path to the primary output. In the case of tie, follow the alphabetical order.*

Based on above algorithm, following table is generated as shown

Step No.	Objective	Action (Backtrace or Backtrack)	Implied Values of PI	Implied signal values	D-frontier	X-path

3B. Apply SCOAP to **Figure 3B**.

3C. Apply Fault equivalence and Fault dominance rule for the circuit shown in **Figure 3C**.

(4+3+3)

4A. Consider the BILBO circuit as shown in Figure 4A. Explain all modes. What will be the output (Q0, Q1, Q2, Q3) when inputs are 1001 and control signals are B1=1,B2=0 ?

4B. Consider the Function, F(a ,b, c)= a b + b c' with SA1 fault in a. Find the spectral coefficients.

4C. (i) Testing targets……

(ii) A quantity to measure quality of a test set is……..

(iii) Three modes of operation in scan are……

(4+3+3)

5A. Apply scan path technique and ATPG, to find the T.V. in **Figure 5A**.

5B. (i) Replace block G with a 3 i/p logic gate such that the following circuit becomes a complete LFSR as shown in **Figure 5B**.

(ii) Which of the following statements is false?

a) Power consumption of a circuit is lower in normal mode than in test mode.

b) Test power depends on successive test patterns.

c) DFT circuitry is utilized more in normal mode than in test mode.

d) Switching activity of nodes of a circuit is more in test mode than in normal mode.

5C. Explain about the DSP Based Analog Tester.

(4+3+3)

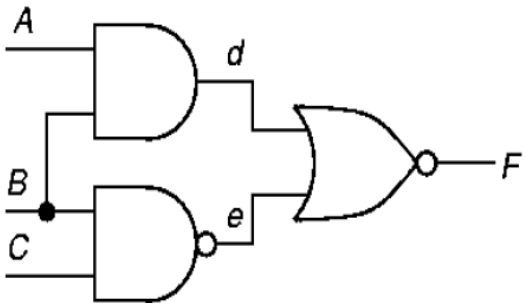

Figure 1B.

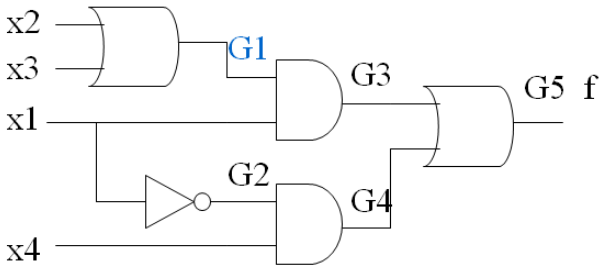

Figure 1C.

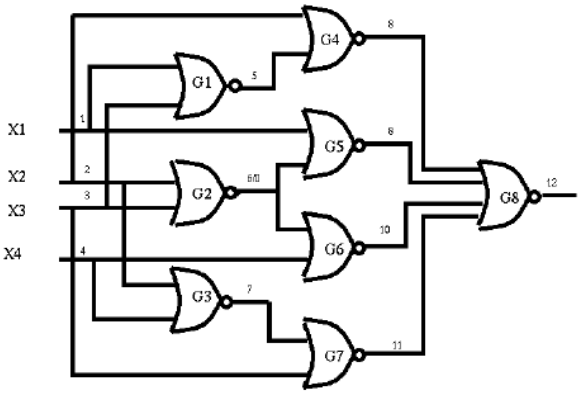

Figure 2B.

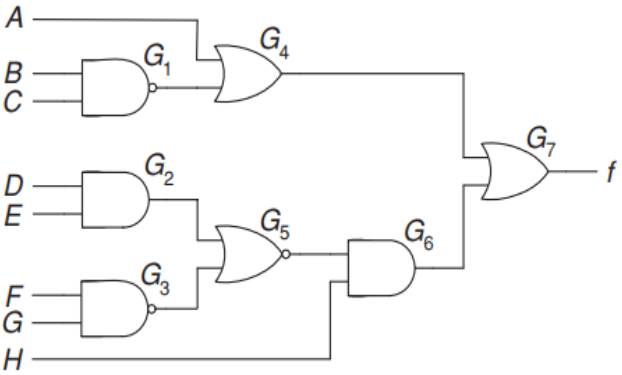

Figure 2C

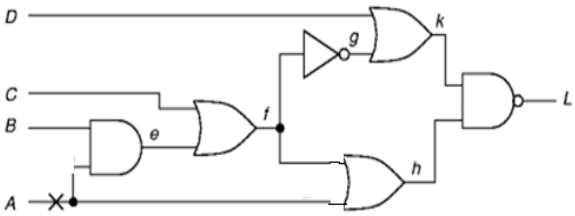

Figure 3A.

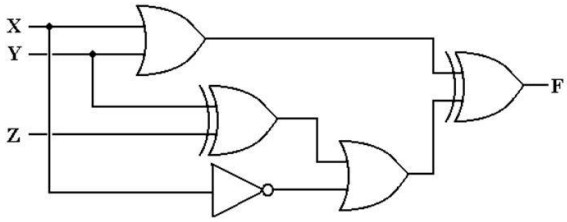

Figure 3B.

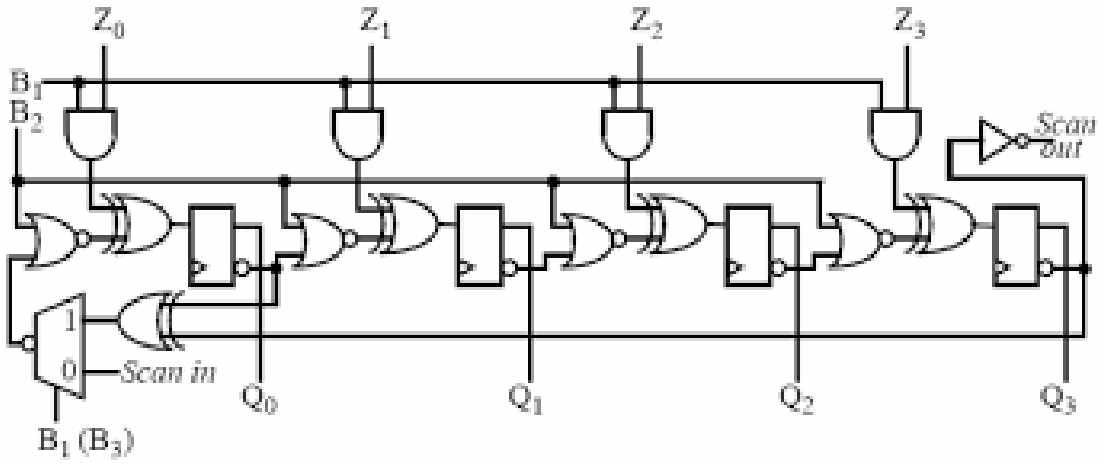

Figure 4A.

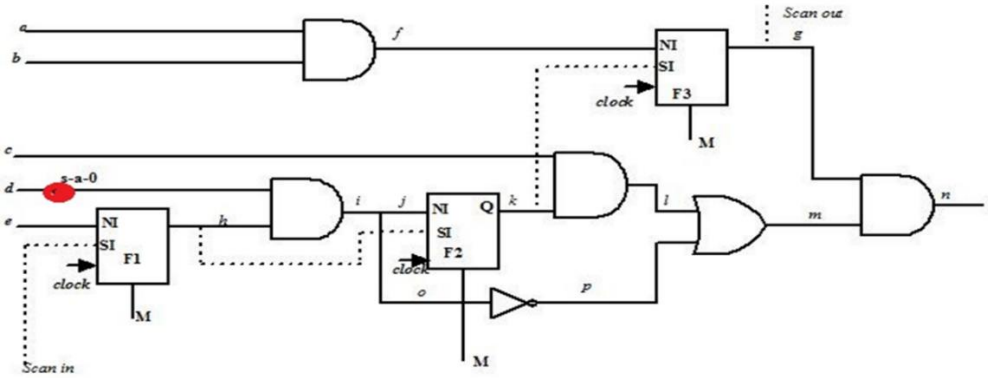

Figure 5A.

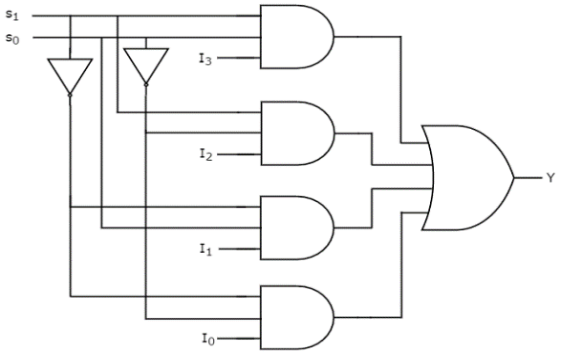

Figure 3C.

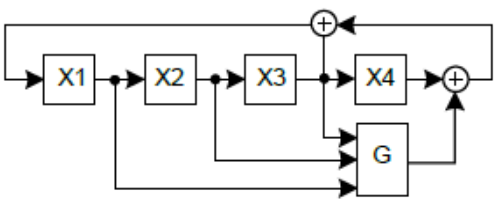

Figure 5B