Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

VI SEMESTER B.TECH. (ELECTRICAL & ELECTRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, APRIL / MAY 2019

SUBJECT: EMBEDDED SYSTEM DESIGN [ELE4001]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 03, MAY 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Support all your programs with relevant comments

1A. i. Discuss the limitations of using clock speed and instructions executed per unit time as the parameters to measure and compare the processing power of processors. Illustrate with relevant examples.

ii. Describe in detail the Dhrystone benchmark. Name the benchmark developed by EEMBC as an alternative to this benchmark. ***(04)***

1B. Show the connection diagram to connect '8' LEDs to port 'B' and 8 keys (push button) to port 'C' of PIC16F877. Write an ALP to keep all the 8 LEDs in off position initially, monitor the switch status continuously and when a key is closed, turn on the corresponding LED (if key connected to RC0 is closed, LED connected to RB0 should be turned on and so on). Keep the LED on for a suitable time and then turn it off and continue monitoring the switch status. ***(04)***

1C. Write equivalent ARM assembly code for the following 'C' program. Use suitable registers and memory locations.

```
unsigned int num[100] = {0x12345678, 0xA0305070, ---------- };
int  sum =0;
for (int i=0; i<100; i++)
{
    sum+=num[i];
}
```

(02)

2A. What do you mean by pipeline flush? When does this occur? Illustrate with the help of a relevant example with respect to '3' stage pipeline in ARM7TDMI. Suggest methods normally used to minimize pipeline flushing. ***(03)***

2B. Write an ARM7TDMI subroutine to determine the ASCII codes for the upper and lower nibbles of an '8' bit number. Assume the '8' bit number to be passed to the subroutine through D_7 to D_0 bits of R0 register (remaining 24 bits are zero). Return the result through registers R1 and R2. (Hint: If the nibble value is between 0 and 9 add 30H and if it is between 'A' and 'F' add 37H to get the ASCII code). ***(03)***

2C. Explain the following with respect to data abort exception.

i. When does this exception occur?
ii. What is the main reason for having this exception in APM7TDMI?
iii. What is the expected operation in data abort exception handler?
iv. Mention and describe the instruction used to return from data abort exception handler.
v. Discuss the reason for using this instruction to return. ***(04)***

3A. Show the interfacing circuit to interface two common cathode seven segment LED display devices to pins 'p11 to p18' and 'p20 to p27' of mbedNXPLPC1768 microcontroller. Write a 'C' code to display the following characters continuously on the display devices with a delay of 3.2 seconds.

EC, 40, FL, IT, 53. ***(04)***

3B. Describe the following with respect to Cache memory

i. Need for cache memory.
ii. Necessity of a replacement policy.
iii. Write through and write back techniques. ***(03)***

3C. With the help of a relevant timing diagram, explain PCI bus protocol for I/O write operation to transfer four '8' bit data in the data field. Assume that no wait cycles are required in case of data '1' and '3'. Target requests for two wait cycles for data '3' and initiator requests for one wait cycle during data '4'. Assume that the target device takes three cycles to respond to the address sent by the initiator. ***(03)***

4A. Write a 'C' program for PIC16F877 microcontroller to configure the MSSP in I2C master mode to transmit data bytes 3AH and 7BH to slave device '1' with address 4CH and then (before stop condition is issued) transmit data bytes 00H and FFH to slave device '2' with address 7FH at a baud rate of 1Mbps. Assume fosc = 20MHZ. ***(04)***

4B. i. Describe the bus arbitration scheme (CSMA / CD) used by CAN serial communication bus to support multi master configuration.
ii. Illustrate the scheme clearly with respect to four nodes (node 10, 11, 12 and 13) initiating communication on CAN bus simultaneously with message IDs; 20CH, 203H, 201H and 232H respectively. ***(03)***

4C. Explain the following with respect to USB serial communication.

i. Connection of devices using tiered, star topology.
ii. Configuration/ enumeration process.
iii. Number of wires, data transfer rate and type of communication possible with USB 2.0 ***(03)***

5A. i. If the analog input applied to AN0/RA0 pin of pic16F877microcontroller is 3.45V, determine the values of ADRESH and ADRESL registers, at the end of conversion. Assume left justified result, positive and negative reference voltages as 4.5V and '0' V respectively.
ii. Write a 'C' program to convert the analog input applied to RE0 / AN5 pin of PIC16F877 microcontroller and display the result at ports 'B' and 'D'. Use right justified result, conversion time of 76.8µs, positive and negative reference voltages from RA3 / AN3 and V_{SS} pins. All the remaining pins of ports A and E should be available as analog input pins. Take F_{osc} = 5MHz. ***(04)***

5B. With the help of relevant diagrams, describe the working of serial IR, IrDA protocol. Explain clearly the role of IR encoder/decoder and IR transceiver. ***(03)***

5C. List the various metrics to be optimized while designing an embedded system and describe in detail the time to market design metric. ***(03)***