Reg. No. | | | | | | | | | | |

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATION, JUNE - 2019

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 4001]

TIME: 3 HOURS MAX. MARKS: 50

Instructions to candidates :*Answer ALL questions and missing data may be suitably assumed.*

1A What is the size of the smallest ROM that is needed to implement the following?

(a) A 4-to-1 MUX

(b) An 8-to-3 priority encoder

1B Find a minimum-row PLA table to implement the following functions:

x(A,B,C,D) = Σm(3, 6, 7, 11, 15)

y(A,B,C,D) = Σm(1, 3, 4, 7, 9, 13)

z(A,B,C,D) = Σm(4, 6, 8, 10, 11, 12, 14, 15)

1C Write a VHDL code to develop a half adder using data flow model. Using this as a component, build four-bit full adder. Draw logic/block diagram wherever required.

(2+3+5)

2A Evaluate: A & NOT B AND C SRA 3 XOR D. Determine the resulting value.
where A = “110”; B = “000”; C = “111000”; D = “110110”.

2B Write a VHDL code for the combinational circuit as shown in Fig. Q 2B using conditional assignment statement.

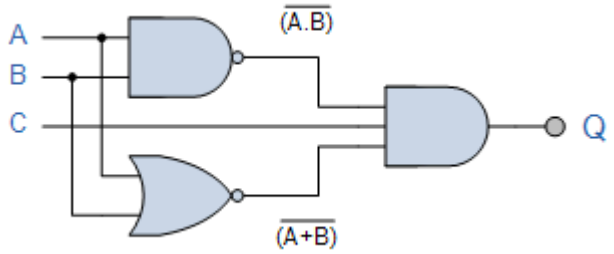

Fig. Q2B

2C Briefly outline the purpose of the following VHDL modelling constructs.

i) Signal attributes
ii) function declaration
iii) component declaration and instantiation
iv) package declaration
v) Generics

(2+3+5)

3A Draw a state graph and state table to implement a sequence detector for detecting a sequence "1101" (overlapping method) using mealy machine.

3B What are the different wait statements available in VHDL? Mention their use with examples.

3C With a state graph, write and explain the VHDL code for traffic light controller realization in PAL22V10.

(2+3+5)

4A Explain SRAM and Anti-fuse programming technology used to make the FPGAs field programmable.

4B Explain the concept of test bench for the verification of design through simulation.

4C How to attach a package to the VHDL module? Explain with an example.

(4+3+3)

5A Explain the architecture of Xilinx Spartan FPGA with a suitable diagrams.

5B Find a minimum set of tests that will test all single stuck-at-0 and stuck-at-1 faults in the network shown in Fig. Q5B.

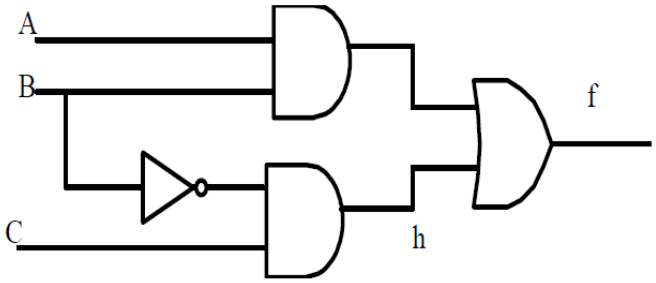

Fig. Q5B

5C Explain testing of sequential logic using scan path testing.

(4+3+3)

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