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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATION, APRIL/MAY - 2019

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 4001]

TIME: 3 HOURS MAX. MARKS: 50

Instructions to candidates :*Answer ALL questions and missing data may be suitably assumed.*

1A What you mean by hazards in combinational networks. Explain its type.

1B Implement a full subtractor using PAL and draw the diagram when the PAL is not programmed and when it is programmed.

1C Briefly explain the FPGA design flow with a neat diagram.

(2+3+5)

2A List various operators in VHDL and give their order of precedence.

2B Write a VHDL program to detect prime number of a 4-bit input using behavioural style of modeling.

2C Write a structural VHDL code to implement Gray to Binary code converter. Use 2 input Exclusive OR gate entity as component.

(2+3+5)

3A Translate the following code to a when…else statement.

```
process(a,b,j,k)
begin
if a='1' and b='0' then
step<="0100";
elsif a='1' then
step<=j;
elsif b='1' then
step<=k;
else step<="0000";
end if;
end process;
```

3B Create a parameterized entity declaration and architecture body pairs using generics for N input multiplexer.

3C A Moore sequential machine with two inputs and one output has the following state table:

PRESENT STATE	NEXT STATE X1X2= 00	01	10	11	OUTPUT (Z)
1	1	2	2	1	0
2	2	1	2	1	1

Write VHDL code that describes the machine at behavioral level.

(2+3+5)

4A Differentiate signal assignment & variable assignment with VHDL programs. Highlight the

corresponding simulation output.

4B Explain the concept of test bench for the verification of design through simulation.

4C Explain the structure of CLB in Xilinx Spartan IIE, highlighting its modes of usage. Explain the technology used to make it field programmable.

(4+3+3)

5A Explain check point theorem with example. Determine the necessary inputs to the Fig. Q5A to test for s-a-0 and s-a-1 faults at h.

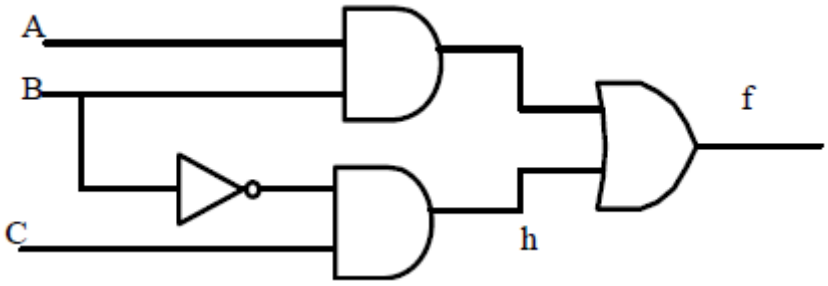

Fig. Q5A

5B Explain the architecture of ACTEL Axcelerator logic modules.

5C With the help of block diagram, explain Boundary scan test.

(4+3+3)

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