Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

III SEM B.Tech (BME) DEGREE END-SEMESTER EXAMINATIONS, NOVEMBER 2019.

SUBJECT: ANALOG ELECTRONICS (BME 2151)
(REVISED CREDIT SYSTEM)
Friday, 15th November, 2019, 8.30 AM to 11.30 AM

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer ALL questions.**
2. **Draw labeled diagram wherever necessary**
3. **Assume suitable data, if missing**
4. **Refer to the table of standard resistors/capacitors (if required)**

1. (A) For the network shown in figure Q1(A), making use of graphical method, determine: 5
   a. I_{DQ} and V_{GSQ}
   b. V_D
   c. V_S
   d. V_{DS}
   e. V_{DG}

   (B) A crystal has the following parameters: L = 0.33H, C = 0.065pF , $C^{|}$ = 1.0pF and R = 5.5 KΩ 3
   (i) Compute the series and parallel resonant frequencies of the crystal
   (ii) What is the Q-factor of the above crystal?
   (iii) By what percentage does the parallel resonant frequency exceed the series resonant frequency?

   (C) Make a comparison of RC coupled Class-A and Class-B Push-Pull power amplifiers. 2

2. (A) For the circuit shown in figure Q2(A), prove that 5
   (a) $Z_i = R_s \,||(1/g_m)$
   (b) $A_v = g_m R_D$

   (B) Determine R_D and R_S for the network shown in figure Q2(B), to establish a gain of 10 using a relatively high g_m at $V_{GSQ} = V_P/4$. Assume $y_{os} = 0$. 3

   (C) Calculate g_{mo} and g_m of a JFET having I_{DSS} =10mA and V_P = - 5V when operated at a d.c bias point of V_{GSQ} = - 2V. 2

3. (A) Prove that for a Class-B power amplifier, the power output $P_{O(\max)} = \frac{V_{CC} I_{C(Sat)}}{4}$ and efficiency $\eta = 78.5\%$. 5

   (B) For the JFET circuit shown in figure Q3(B), considering the dynamic drain resistance calculate the voltage gain with: 3
   (a) Resistor R_S bypassed by a capacitor
   (b) Resistor R_S un-bypassed

(C) The JFET circuit shown in figureQ3(C) has an operating point defined by V_{GSQ} = -2 V and I_{DQ} = 5.625 mA, with I_{DSS} = 10 mA and V_P = -8 V. The applied signal is V_i and y_{os} = 40 µS. 2

(i) Draw a labelled a.c equivalent circuit

(ii) Determine the output resistance "Z_O"

4. (A) For the MOSFET circuit shown in figure Q4(A), having I_{DQ} = 6.7mA and V_{GSQ} = 12.5V, and g_{os} = 20µS. Compute trans-conductance, dynamic drain resistance, input impedance, output impedance, and the voltage gain. 5

(B) Prove that the circuit shown in figure Q4(B) is a unity gain amplifier. 3

(C) Determine the voltage gain and output impedance of the FET amplifier circuit shown in figure Q4(C). 2

5. (A) In a common emitter transistor amplifier circuit, the bias is by a self-bias, and the various parameters are: V_{CC} = 16V, R_C = 3KΩ, R_E = 2KΩ, R_1 = 56KΩ, R_2 = 20KΩ and α = 0.985 and the transistor is made of germanium. Determine (a) Operating point and (b) Stability factor. 5

(B) Calculate the ac output power of the amplifier circuit shown in figure Q5(B). (Assume V_{BE} = 0). 3

(C) Design a current-series feedback amplifier to have an overall trans-conductance gain of -1mA/V, a voltage gain of -4, and a de-sensitivity of 50. Make use of a NPN type BJT having h_{fe} = 150, and assume a signal source with a resistance of 1KΩ. Draw the labelled circuit diagram of the designed amplifier. 2

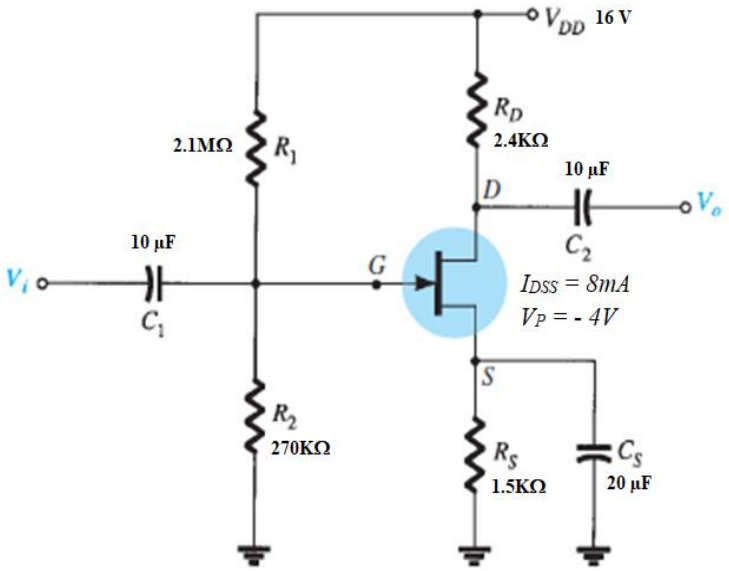

Fig. Q1(A)

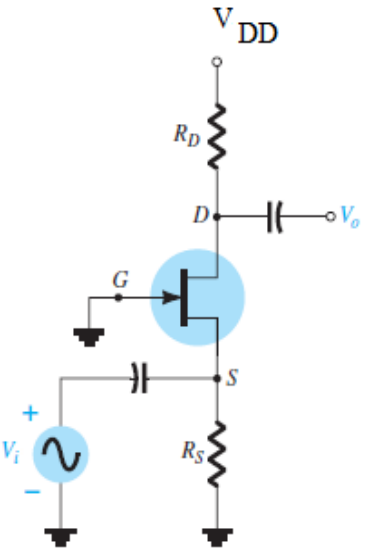

Fig. Q2(A)

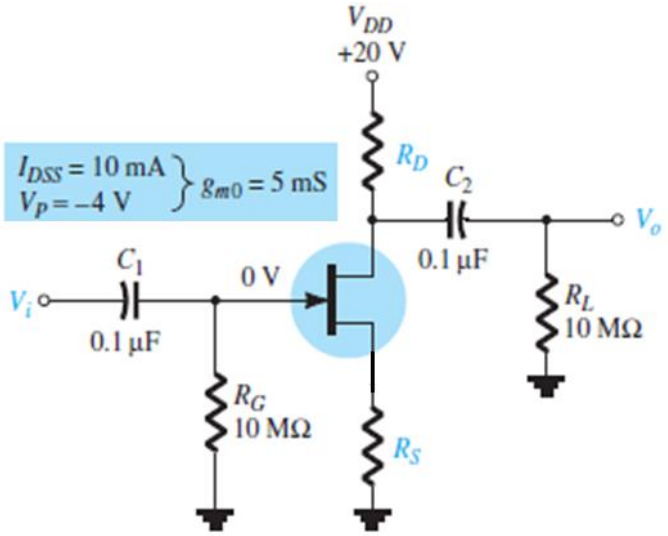

Fig. Q2(B)

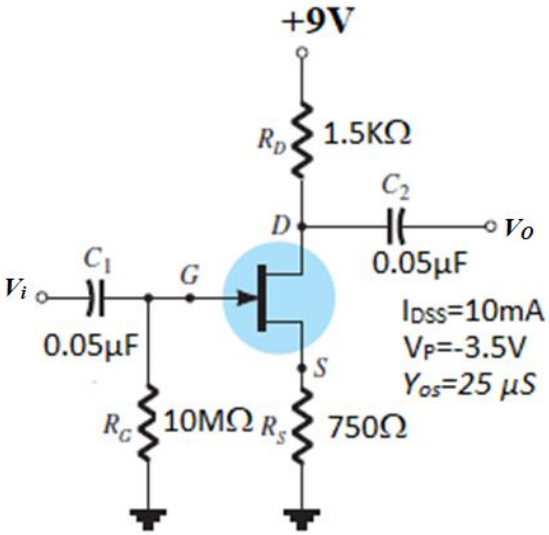

Fig. Q3(B)

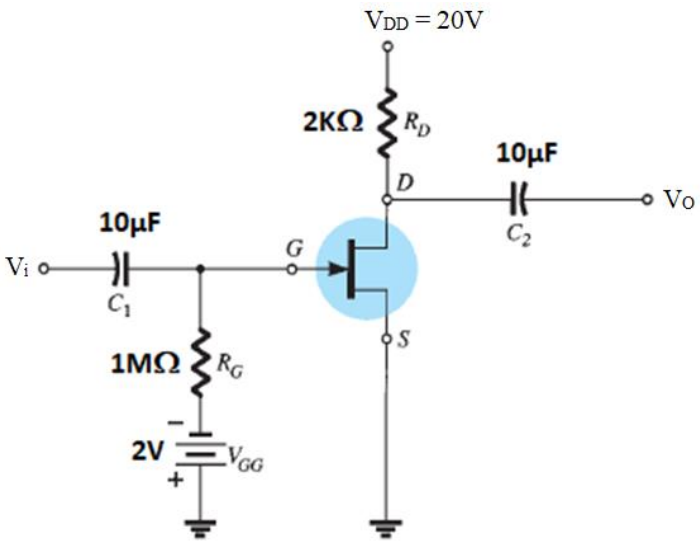

Fig. Q3(C)

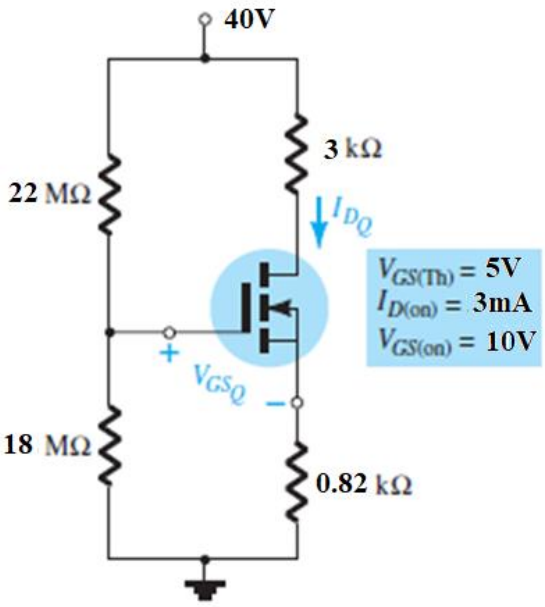

Fig. Q4(A)

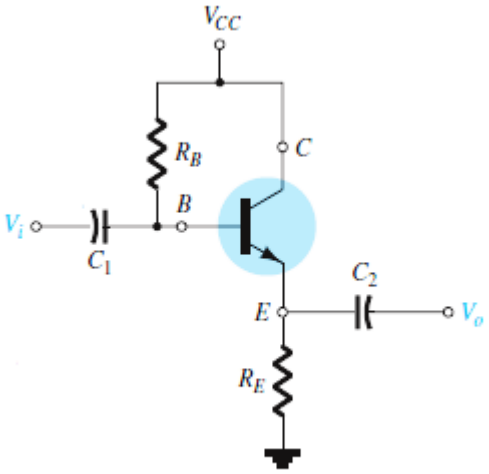

Fig. Q4(B)

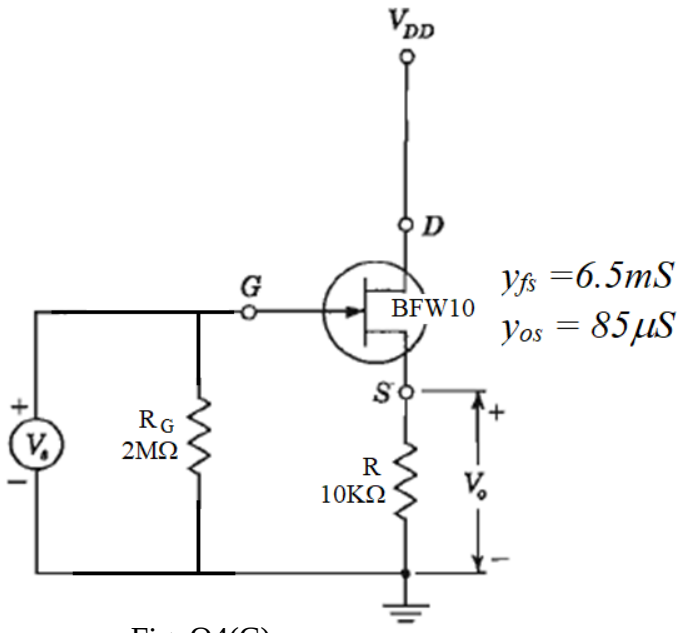

Fig. Q4(C)

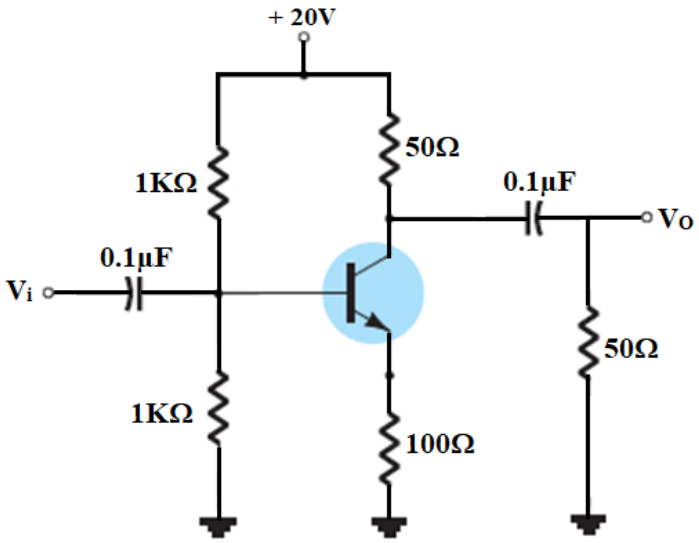

Fig. Q5(B)