Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

III SEM B.Tech (BME) DEGREE END SEMESTER EXAMINATIONS, NOVEMBER 2019

SUBJECT: DIGITAL ELECTRONICS (BME 2153)
(REVISED CREDIT SYSTEM)
Thursday, 21st November, 2019: 8.30 AM to 11.30 AM

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. Answer ALL questions.
2. Draw labeled diagrams wherever necessary.

1A. Depicting the necessary steps and calculations perform the following: 04

$(a) Add\ using\ BCD\ code$

$(i)\ 75 + 38$
$(ii)\ 197 + 184$

$(b)\ Convert\ into,$

$(i)\ (36)_8 = (\ \ )_{10} = (\ \ )_{16}$
$(ii)\ (A32)_{16} = (\ \ )_{10} = (\ \ )_8$

1B. Simplify the following functions to a minimum number of literals using Boolean simplifications. 03

$(i)\ F(x, y, z) = xyz + \bar{x}y + xy\bar{z}$

$(ii)\ F(w, x, y, z) = y(w\bar{z} + wz) + xy$

$(iii)\ F(x, y, z) = (xy + z)(y + xz)$

1C. Realize the following Boolean function into (i) Sum of Min-terms. (ii) Products of Max-terms. 03

$F(A, B, C) = AB + \bar{A}C$

2A. Draw the circuit of a 4 bit parallel adder/ 2's complement positive difference subtractor using the IC 7483. Explain the operation of the circuit with suitable examples. 04

2B Obtain the simplified Boolean expression for the following Boolean function using Karnaugh map. Also simplify the expression without using don't cares, and realize using basic gates. 03

$$f(A,B,C,D) = \sum m\,(0,2,4,5,6,7,8) + \sum d\,(10,11,12,13,14)$$

$$d \rightarrow don't\ cares$$

2C. What is a De-multiplexer? Realize and draw the circuit of 1×4 line De-multiplexer with active low outputs. 03

3A. Realize and draw the circuit of a full adder using 3×8 line decoder with appropriate gates. 04

3B. Realize and draw the circuit of 2 bit magnitude comparator. 03

3C. Draw the circuit of a D flip flop using appropriate gates. Give its complete truth table and obtain its excitation table. 03

4A. Realize Octal numbers (0 to7) to seven segment display using ROM circuit. Draw the complete circuit. 04

4B. Design a 4×1 MUX to realize the following function. 03

$$F(A,B,C,D) = \sum m(0,2,3,5,7,10,11,12,14,15$$

4C Design and draw an Encoder using diode matrix to satisfy the following truth table. 03

Inputs				Outputs			
w_3	w_2	w_1	w_0	y_3	y_2	y_1	y_0
0	0	0	1	1	0	1	1
0	0	1	0	0	1	0	1
0	1	0	0	1	0	1	0
1	0	0	0	0	1	1	1

5A. Design a synchronous counter to count the following count sequence using JK flip flops. Also verify the counting with timing waveforms. 04

$000, 001, 010, 100, 110, 111, 000, \ldots \ldots$

5B. Draw the circuit of a 3 bit shift register using D flip flops to operate as (i) PIPO (ii) PISO. Explain the operation with the appropriate truth table. 03

5C. Draw the circuit of a Mod-11 asynchronous counter. List the count sequence and draw the timing waveforms. 03