Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV 2018

COMPUTER ORGANIZATION AND DESIGN [CSE 2101]

REVISED CREDIT SYSTEM
(20/11/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Consider two 2's complement numbers A = +128 and B = -128. Perform addition as A + B and subtraction as A – B on these two numbers. Give the values of Carry flag, Negative flag, Overflow flag and Zero flag after addition and subtraction. **3M**

1B. Write a CISC program to find the average of N numbers stored in successive word locations in memory. **4M**

1C. Consider a computer (C1) that has a byte-addressable memory organization in 32-bit words according to Big-endian scheme and another computer (C2) that adopts little-endian scheme. A program stores the string "ABCDEFG" entered at the keyboard in successive byte locations starting at location 1000. Show the contents of two memory words at locations 1000 and 1004 in the computers C1 and C2. **3M**

2A. Design a 4-bit ALU that is capable of performing operations on the 4-bit operands A and B to meet the specification as given in Table Q. 2A

Table Q. 2A

S1	S0	Output Z
0	0	A plus B
0	1	A minus B
1	0	A AND B
1	1	$\bar{A}$

Draw the separate diagrams for the organization of 4-bit arithmetic unit, 4-bit logic unit and combining the outputs generated by the arithmetic unit & logic unit while designing. **5M**

2B. Perform the fast multiplication operation as it would be computed using bit-pair recoding of the multiplier to multiply +13 with -6. **3M**

2C. Verify your answer obtained in question 2B, using Booths recoded multiplier. Compare both the methods and give your justification. **2M**

3A. For the state diagram given in Fig. Q.3A, draw a controller using sequence controller, counter and decoder. Also explain its working.

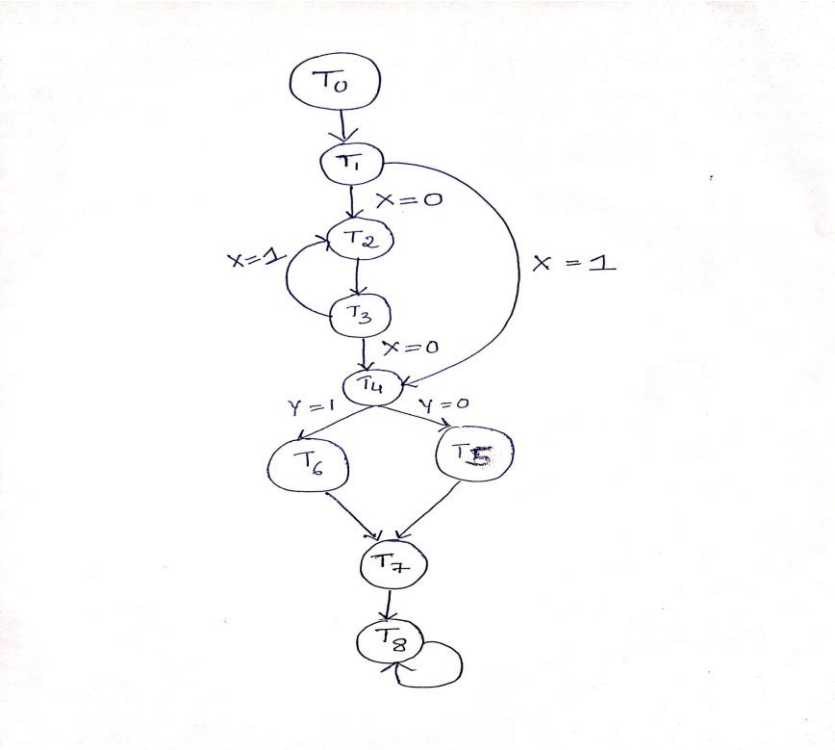

Fig. Q. 3A

5M

3B. Write the truth table for the sequence controller of the controller in question 3A. **3M**

3C. List the differences between Hardwired and microprogrammed approach of Control unit. **2M**

4A. Construct a larger memory module of 2M words of 24-bits each using 512K X 8 static memory chips. Explain its working principle. **3M**

4B. For a direct-mapped cache design with a 32-bit address and byte-addressable memory (1 word = 8 bytes), if a cache block size is 8 words and cache memory has 32 blocks, what is the number of bits in tag, block, word fields? **3M**

4C. Define seek time and rotational latency. In a disk system there are 25 recording surfaces. The diameter of each recording surface is 30 cm and the inter track distance is 0.05 cm. All the disks are 2 sided disks except for one disk. There is an average of 360 sectors per track and each sector contains 512 bytes of data.

(a) How many tracks will be there in a two sided disk?

(b) How many cylinders will be there in the entire system?

(c) What is the total capacity of the disk system? **4M**

5A. Explain memory mapped I/O and I/O mapped I/O. With the neat diagram also explain I/O interface for an input device. **4M**

5B. Explain with a neat diagram keyboard to processor and processor to display connection. **4M**

5C. What are vectored interrupts? Explain. **2M**