Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

MAKE-UP EXAMINATIONS DEC-2018

SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]

REVISED CREDIT SYSTEM
(23/11/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer ***ALL*** the questions.
- Missing data may be suitably assumed.
- All the inputs are available only in ***true*** form.

1A. Obtain the simplified SOP and POS expression for the following function using algebraic manipulation. **3M**

$F(a,b,c,d)=\pi M(1,3,6,10,11,12,13,14)$

1B. Find all the essential prime implicants, and the minimum cost SOP expression for the function, $F(a,b,c,d)=\sum m(1,3,4,5,10,11,12,13,14,15)$ using K map. Implement the minimum cost SOP using only NOR gates. **3M**

1C. A circuit with two outputs has to implement the following functions **4M**

$F1(a,b,c,d)=\sum m(0,2,4,6,7,9)+D(10,11)$

$F2(a,b,c,d)=\sum m(2,4,9,10,15)+D(0,13,14)$

Design the minimum cost circuit and compare its cost with combined costs of two circuits that implement F1 and F2 separately.

2A. Design an arithmetic comparison circuit which takes two 5 bit binary numbers A and B as inputs and gives three single bit signals AltB, AeqB and AgtB as outputs. **3M**

2B. Write the Verilog code for an n bit ripple carry adder with carryout using ***for*** loop. **3M**

2C. Using only full adders and other necessary gates, design and write the Verilog code for a circuit which takes two 4 bit signed numbers A and B as input and gives three single bit outputs Z, N and V after performing the operation 'A-B'. The three outputs are obtained as per the conditions given below: **4M**

- If 'A-B' is 0 then Z=1 else Z=0.
- If 'A-B' is negative then N=1 else N=0
- If arithmetic overflow occurs then V=1 else V=0.

.

3A. Design and write the Verilog code for a 3 to 8 decoder using 2 to 4 decoders and other necessary gates. Use ***case*** statement to implement 2 to 4 decoder. **4M**

3B. Write the truth table for 2421 to 8421 code converter. Design and write the Verilog code for this converter using 4:1 multiplexer(s) and other necessary gates. Write behavioral Verilog code to implement the same. Use ***conditional*** operator to implement 4:1 multiplexer. **4M**

3C. Using Shannon's expansion, design and implement the function $f(A,B,C,D)=\sum m(1,5,7,8,14)$ with 4:1 multiplexer and other necessary gates. Assume A and B as the select signals for the 4:1 multiplexer. **2M**

4A. Write the characteristic and excitation table for JK, RS, D and T flip-flop. **4M**

4B. A sequential circuit has two JK flip-flops A and B, one input x, and one output y. It is described by the following output and flip-flop input functions. **4M**

JA=(Bx')' JB=((AB')'(Bx)')'

KA=(A'+B)' KB=JB Y=(ABx')'

Draw the state table and state diagram.

4C. Draw the logic diagram of a 4 bit register with four D flip-flops and four 4:1 multiplexers with selection inputs S1 and S0. The register operates according to the following function table. **2M**

S1	S0	Register operation
0	0	No change
0	1	Complement the 4 outputs
1	0	Clear register to 0
1	1	Load parallel data

5A. With a neat diagram explain the working of NMOS realization of a NAND gate. **3M**

5B. i. Explain the general structure of PLA with a neat diagram. **(2+2)M**

ii. Define Noise margin. Write down the equations for low and high noise margins.

5C. What is inverting and non-inverting buffer? Design and explain the working of a CMOS non-inverting buffer. **3M**