Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKE UP EXAMINATIONS, DECEMBER 2019

DIGITAL SYSTEM DESIGN [ELE 2152]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 23 DECEMBER 2019** **Max. Marks: 50**

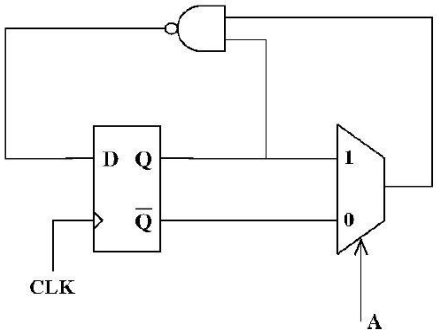
Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Two motors M1 and M2 are controlled by three sensors, S3, S2 and S1. One motor M2 is to run anytime when all three sensors are ON (true) as well as when any two sensors are ON (True). M2 is also ON when only S3 is ON. The Motor M1 is to run whenever sensors S2 or S1, but not both, are ON. When all three sensors are OFF then both motors must remain OFF. Construct a truth table and write the Boolean output equation for the given specification. Implement the circuit using NAND-NAND realization method. ***(03)***

1B. Design a 4 bit binary code to gray code converter using active high 3:8 decoders. Residual gate may be used. ***(05)***

1C. Draw the state diagram of the following figure.



(02)

2A. Simplify the following expression using VEM method and obtain the minimal SOP form, consider z as the MEV

$$f(v,w,x,y,z) = \sum m(1,4,6,7,9,15,16,18,19,22,24,25,28,29) + d(2,3,8,17,27,31)$$

(05)

2B. Realize the Boolean expression $f(w,x,y,z) = \sum(0,2,4,5,7,9,10,14)$ using multiplexer tree structure. The first level should consist of two 4 to 1 line multiplexer with the variable w and z on their select line S1, S0 respectively and Second level should consist of single 2 to 1 line multiplexer with the variable y on its select line. ***(03)***

2C. State the importance of Valid bit in 4 to 2 Priority encoder, with the help of relevant truth table. ***(02)***

3A. Design a comparator using 4 bit binary parallel adder IC (IC 74283) and residual gate that compares two 4 bit unsigned number, X3-X0 and Y3-Y0. The comparator has two output G and S. such that G=1 and S=0 if X>Y and S=1 and G=0 if X<Y and G=S=0 if X=Y. ***(05)***

3B. Design a presettable ripple down counter using JK flip flop, which has the states 6-5-4-3-2-6-.. repeats. ***(03)***

3C. Briefly explain the flip flop timing characteristics. ***(02)***

4A. Develop a circuit to generate the sequence 15-7-14-13-11-6-3-1-2-9-12-15-7-…..using universal shift register IC. ***(05)***

4B. Discuss the Verilog HDL modeling styles with illustration. ***(03)***

4C. Design a digital circuit which generates the pattern 1100-0110-0011-1001-……. repeats using D flip flops only. ***(02)***

5A. Draw the state diagram of a sequence detector with serial input w and output z. The output z will be asserted 1 when '00' or '11' is received as continuous data else z=0. Realize the detector as moore machine and implement the circuit using T flip flops, design the next state decoder and output decoder with 8:1multiplexers. (Consider the present state of the flip flop as select lines for multiplexers) ***(05)***

5B. Convert JK flip flop to T flip flop. ***(03)***

5C. Design a frequency divider circuit to generate a 1Hz square pulse, using binary counter IC. Let the input clock frequency of the system is 256Hz. ***(02)***