MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent institution of MAHE, Manipal)

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, NOV 2019
SUBJECT: DIGITAL SYSTEM DESIGN [MTE 2152]
CREDIT SYSTEM
(21/11/2019)

1A	Apply VEM technique, and simplify the following expression, to obtain a minimal SOP expression. F(A,B,C,D,E) = ∑m(3,5,14,19,20,21,22,24,25,28,29) + d(1,2,6,7,10,16,17,23,30)where E is the MEV.	5	CO1
1B	Design a 4 to 2 Priority Encoder using gates.	3	CO2
1C	Draw the flow chart for the Digital System Implementation option	2	CO4
2A	Design a binary to Gray code converter using dual 4 to 1 multiplexers (74x153).	5	CO2
2B	List the properties need to be possessed by programming elements of an FPGA. Also list the 4 programming elements of an FPGA, mentioning the differences between them.	3	CO4
2C	Demonstrate a 5 to 32 decoder using minimum number of 2 to 4 and 3 to 8 decoders.	2	CO2
3A	Design a synchronous 3 bit binary up / down counter. The counter should count up when the up/down control input G is 0 and count down when G is 1. Implement the circuit using T flip- flops.	5	CO3
3B	Design a circuit to generate 100 KHz clock signal from 6MHz clock signal. Use 74LS93 for implementation.	3	CO3
3C	Sketch the state diagram of JK flip-flop.	2	CO3
4A	Using a 4 bit universal shift register (74LS194) design a sequence generator which cycles through the following sequence. 0-8-12-6-13-11-7-3-1-0-…..	5	CO3
4B	Draw the state diagram (Moore m/c) of a sequence detector which has a single input x and a single output z. The output variable z will be asserted if it detects a sequence of two 0's followed by 3 bits which consists of a single 1.	3	CO3

4C Draw the output waveforms (Q1, Q2) of the circuit given in Figure Q12.

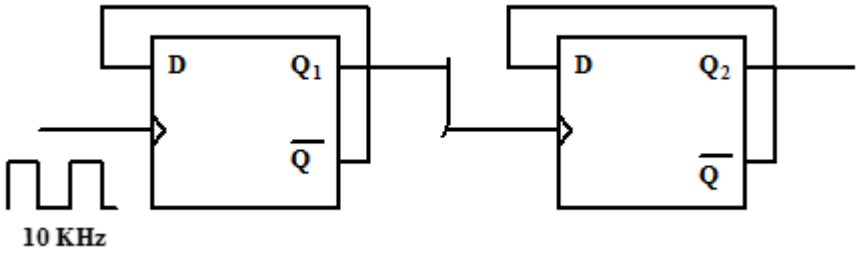

Figure 4C

2 CO3

5A A sequential circuit with two D Flip flops A & B, one input X and one output Z specified by the following equations.

$$D_A = x;\ D_B = Q_A + \bar{x};\ Z = \bar{Q}_A Q_B \bar{x} + Q_A Q_B x$$

a. Draw the logic diagram of the circuit
b. Derive the state table
c. Draw the state diagram
d. Identify the objective of the problem

5 CO3

5B Write a data flow Verilog code for a 1 bit full adder. Using this as a component write a structural Verilog code for a 4 bit full adder. 3 CO5

5C Write a gate level Verilog code for a 4 to 1 multiplexer 2 CO5