Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

V SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2019

SUBJECT: COMPUTER ARCHITECTURE [CSE 3101]

REVISED CREDIT SYSTEM
(14/11/2019)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. List and explain Flynn's classification of computer system. **3M**

1B. What are the different data hazards introduced due to out-of-order execution of the following code sequence? Identify and demonstrate possible hazards that can be resolved. **3M**

```
A:   L.D     F0, 0(R1)   //L.D: Load the first element in array 0(R1) to F0
B:   MUL.D   F4, F0, F2  //MUL.D :Multiply
C:   S.D     F4, 0(R1)   //S.D: store F4 in 0(R1)
E:   L.D     F0, 0(R1)
F:   MUL.D   F4, F0, F2
G:   S.D     F4, 0(R1)
```

1C. Consider a five-stage pipelined processor specified by the following reservation table in figure 1C. **4M**

	1	2	3	4	5	6	7	8
S1	X						X	
S2		X	X					
S3				X				
S4		X			X			X
S5						X		

Figure 1C. Reservation table

i) List the set of forbidden latencies and the collision vector.
ii) Draw a state transition diagram showing all possible cycles without causing the collision in the pipeline.
iii) List all the simple cycles from the state diagram. Identify the greedy cycles among the simple cycles. What is the MAL of this pipeline?

2A. Define maximum parallelism degree of a computer system. How to find the maximum parallelism degree of a computer system? **2M**

2B. For N number of PEs, prove that an Illiac routing functions are a subset of Barrel shifter routing functions such that, 5 < N < 50. Write all the permutation cycles for this. How will you relate the connectivity of these two networks? With the help of the above permutation cycles prove this relation. **5M**

2C. Design a Multistage Network that has 4, 2x2 switch boxes in each stage and uses Inverse Perfect Shuffle function between the stages. The PEs are directly connected to the switch boxes at the input side. Solve the routing functions by considering all the PEs and write the corresponding permutation cycles. Show the switch settings in the above design for routing a message from node PE_5 to node PE_4. Find another source and destination which creates a block in the above path in the output side of middle stage. Show the switch settings for this in the same design. **3M**

3A. Write an algorithm/pseudocode for calculation of the following: **2M**

S(K) = $\prod_{i=0}^{k} A_i$ for k=0,1,2,……,N-1 for N elements in vector A and same number of PEs in SIMD machine using $\log_2$ N steps.

3B. Draw a neat diagram of an Intel X86 multicore product that uses superscalar cores. Explain all the components that are shared by each core in this product. **4M**

3C. Explain the organizational changes involved in processor design to increase instructional level parallelism. What are the advantages of a shared L2 cache on the chip over dedicated caches in multicore products? **4M**

4A. With the help relevant diagrams, justify the following: **4M**

(i) Does write policy/policies result in inconsistency of the data?

(ii) Does multiprocessing yield a greater performance when compared with multiprogramming?

4B. With a neat diagram for each, explain the variations IA-64 processor that has a capability to issue four instructions per cycle. **3M**

4C. Explain the functionalities that a multiprocessor operating system must provide so that a user can construct applications without knowing whether a single processor or multiple processors are available to handle the work submitted. **3M**

5A. Explain in detail the component that has replaced front side bus in intel X86 product that uses shared L3 cache. **2M**

5B. There are 3 processors in a multiprocessor system as shown in the figure 5B. Explain steps followed in the requesting processor and the snooping processor that uses write-invalidate protocol for the scenario given below which is executed in sequence. Draw the state transition diagram for both cases. **5M**

i) Processor 1 wants to write to X in its cache.

ii) Processor 3 reads the value X and Z in its cache.

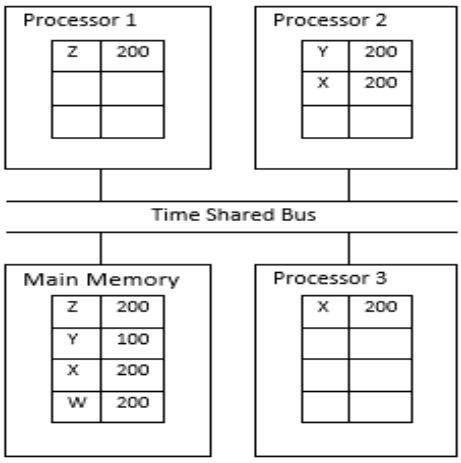

Figure 5B

5C. Explain the blade server architecture and the ethernet configuration for a blade server site. **3M**