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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

V SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER MAKE-UP EXAMINATIONS, DEC 2019

SUBJECT: COMPUTER ARCHITECTURE [CSE 3101]

REVISED CREDIT SYSTEM

(19/12/2019)

Time: 3 Hours

MAX. MARKS: 50

Instructions to Candidates:

- ❖ Answer **ALL** the questions.
- ❖ Missing data may be suitable assumed.

- 1A.** How the efficiency of a linear pipeline is measured? Differentiate between **3M**
 a. Static and dynamic pipelines
 b. Unifunctional and Multifunctional pipelines
- 1B.** Draw and explain the instruction cycle state diagram. **3M**
- 1C.** Consider a 4-stage pipelined processor specified by the reservation table in Table 1C. **4M**

	0	1	2	3	4	5
S1			X		X	
S2		X		X		
S3	X					X
S4		X		X		

Table 1C. Reservation table

- (i) List the set of forbidden and permissible latencies and the collision vector.
 ii) Draw a state transition diagram showing all possible cycles without causing the collision in the pipeline.
 iii) List all the simple cycles from the state diagram. Identify the greedy cycles among the simple cycles. What is the MAL of this pipeline?
 iv) What is the efficiency of this pipeline?
- 2A.** Sort the following numbers in descending order using odd-even transposition sorting using SIMD machine. **3M**
- | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| PE0 | PE1 | PE2 | PE3 | PE4 | PE5 | PE6 | PE7 |
| 21 | 19 | 34 | 12 | 5 | 16 | 92 | 87 |
- 2B.** Design an Omega Network which has 4, 2x2 switch boxes in each stage. Solve the routing functions by considering all the PEs and write the corresponding permutation cycles. Show the switch settings in the above design for routing a message from PE₀ to node PE₆. Find another source and destination which creates a block in the above path in the second stage. **3M**
- 2C.** Explain the four programmatic levels of parallel processing and the potential advantages of simultaneous multiprocessor organization over uniprocessor organization. **4M**

- 3A.** Write an algorithm for SIMD matrix multiplication to multiply two matrices of dimension $n \times n$ where the elements of the matrices are initially stored in the PEM in column-major. Show all the SIMD multiplications carried out in each of the 2 PE's for a 2×2 matrix. Show all the steps clearly. **4M**
- 3B.** Draw a neat diagram of an Intel X86 multicore product having shared L2 cache organization. Explain the components that are dedicated to each core. **3M**
- 3C.** Compare shared L2 cache on the chip over the dedicated L2 caches in the multicore system. **3M**
- 4A.** Why the software performances force Multicore systems as an alternative to the Multiprocessor systems? With neat diagrams explain the general organizations for multicore systems having shared cache organization. **4M**
- 4B.** Explain the process of data transfer and exclusive access in directory protocol. **3M**
- 4C.** Explain how cache consistency is maintained between L1 and L2 caches in simultaneous multiprocessors? **3M**
- 5A.** With a neat diagram for each, explain the variations of the superscalar processors that issues multiple instructions per cycle but only instructions from a single thread are issued in a single cycle. **3M**
- 5B.** Explain how load balancing and parallel computation problems are solved in clusters. **4M**
- 5C.** Give a comparison between clusters and simultaneous multiprocessing. **3M**