Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

V SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV 2019

SUBJECT: FPGA Based Digital System Design [MTE 4014]

(27/11/2019)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Data not provided may be suitably assumed
- Graph sheets will be provided

1A.	Illustrate hierarchical verilog modelling with suitable example. Also develop hierarchical modelling of a 4-bit adder using parameterization and redefine to 16-bit adder after five samples.	**04**	**CO1**
1B.	Develop a verilog program for the Boolean function f=minterms{0,1,5,6,7} using a) Gate level structural modelling. b) Data flow modelling c) Behavioural Modelling	**04**	**CO1**
1C.	Write a Verilog module to generate the waveform as shown in Fig.1c using 50MHz FPGA.	**02**	**CO1**

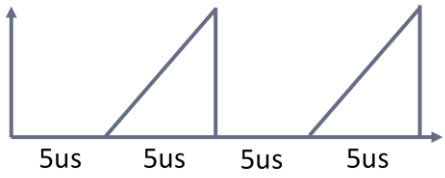

Fig. 1c

2A.	Realize the boolean function depicted in Fig. 2a using PROM and asynchronous PLA AND plane modelling.	**03**	**CO2**

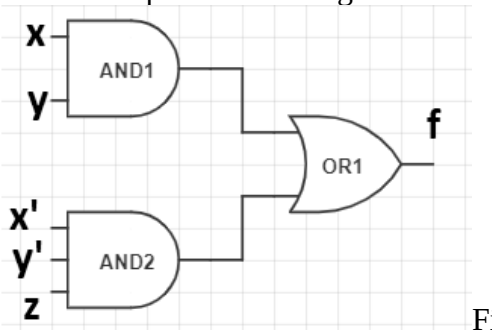

Fig. 2a

2B.	Mention various design options of digital systems and compare them.	**04**	**CO2**
2C.	Demonstrate how FPGA's are suitable for implementation of Finite State Machines and write a verilog module for traffic light system (Red, Yellow, Green) using FSM.	**03**	**CO3, CO4**

3A. Generate the test vectors using Boolean Difference for the logic in Fig. 3a when **03** **CO4**

i) a stuck at 0

ii) a stuck at 1

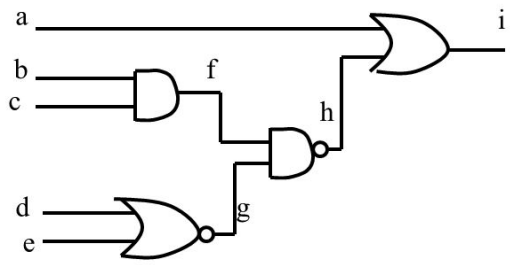

Fig. 3a

3B. Explain the functional behavior of Scan-Flipflop with neat circuit diagram. **03** **CO4**

3C. Summarize the internal structure of XILINX XC4000XL FPGA. **04** **CO3**

4A. Write a Verilog HDL program for synchronous RAM module with size of 32 word lines and each word with byte size. **04** **CO1**

4B. State the design flow steps of FPGA and write a simulation testbench for 4:1 Mux. **04** **CO1, CO3**

4C. Plot the output signals of a 3bit Binary ripple counter with 50kHz clock. **02** **CO1**

5A. A 8-bit microcontroller is to be designed using digital system design with the following functions of Arithmetic & Logic Unit (ALU) as listed below. Microcontroller has two input registers A and B of 8-bit and a synchronous memory of 32lines with 4bit data in each line. **08** **CO4**

Functions

0: A&B, 1: ~A, 2: A+A, 3: A+B, 4: A-B, 5: A=A+1, 6: A=A-1, 7: A^B.
8: Load A with Data 9: Load B with data 10: Clear A 11: Clear B
12: Load B with A data 13: No operation (NOP) 14: Load A with all 1's
15: Load B with all 1's
The result of the output is stored in A always.

i) With the block diagram of Microcontroller and all ALU functions, illustrate how microcontroller works between ALU, Memory and Inputs.

ii) Develop the Verilog model for the microcontroller.
Generate a clock of 20ns with FPGA of 1ns sample. Create a memory within module of microcontroller. Develop provision to read the instructions one by one stored in Memory. Initial start address of memory is 0. It takes 4 clocks to go execute each instruction and go to next memory location.

iii) If the memory has following data stored at the following memory locations
(Memory)0→(data)10, 1→5, 2→5, 3→5, 4→5, 5→6, 6→6, 7→6, 8→6, 9→5, 10→5, 11→5, 12→5, 13→6, 14→6, 15→6
Plot the output value of A with respect to time.

iv) If the following sequence of functions to be required to do, what should be data in memory, final value of A and total time.
Load 5 to A, Load 10 to B, A+A, A-B, A+B, A+1, A-1, ~A, A^B, A&B, ~A, Load B to A, Load 255 to A, A+B, Load 10 to B, A+B, NOP, NOP, NOP

5B. Discuss how to develop a Proportional Integral (PI) controller using FPGA based digital system design. **02** **CO4**