



MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL
(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.) END SEMESTER DEGREE EXAMINATIONS, DECEMBER - 2019

SUBJECT: VLSI DESIGN [ICE 4004]

TIME: 3 HOURS

MAX. MARKS: 50

Instructions to candidates : Answer ALL questions and missing data may be suitably assumed.

- 1A. Illustrate BiCMOS fabrication with figures.
- 1B. Explain how MOS transistor trans conductance and output conductance determine the operation of a transistor.
- 1C. Determine the pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistors.

(4+2+4)

- 2A. The pFET pass transistor in Figure Q2A has an aspect ratio of 8 in a process where $k_p = 60 \mu A/V^2$, $V_{DD} = 3.3 V$, and $V_{Tp} = -0.8 V$. At time $t=0$, the output capacitor is charged to a voltage of V_{DD} while the input is switched to $V_{in} = 0 V$.
 - (a) Find the fall time at the output node.
 - (b) The input is switched back to V_{DD} . Find the rise time needed to drive the output voltage back to its high value.

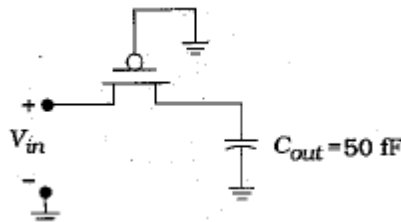


Figure Q2A

- 2B. Consider a complex CMOS logic gate that implements the function $f = \overline{a.b + c.d.e}$. Design the logic circuit by specifying the β_n and β_p values of the FETs in the worst case condition.
- 2C. Sketch a stick diagram of a CMOS logic gate implementing the function $f = \overline{(a.b) + (c.d)}$ and estimate the cell width and height in terms of ' λ '.

(3+3+4)

3A. Calculate the delay in this network shown in Figure Q3A.

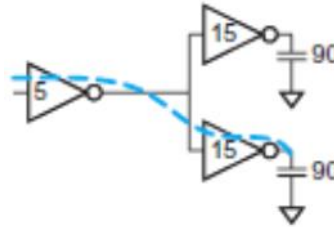


Figure Q3A

3B. Draw the transistor level diagram of a NOR based SR latch.

3C. Briefly explain the design parameters and problems associated with VLSI design.

(2+5+3)

4A. Classify programmable logic devices based on their design.

4B. The following state table is implemented using a ROM and two D flip-flops (falling edge triggered):

Q_1Q_2	$Q_1^+Q_2^+$		Z	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00	01	10	0	1
01	10	00	1	1
10	00	01	1	0

Draw the block diagram and the ROM truth table.

4C. Briefly explain different types of interconnects used in FPGA.

(3+4+3)

5A. Explain different types of FPGA programming technologies.

5B. Illustrate the BIST testing technique with a block diagram.

5C. Briefly explain the Integrated Circuit (IC) packaging families.

(3+4+3)
