Reg. No. | | | | | | | | | | |

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATIONS, NOVEMBER - 2019

SUBJECT: VLSI DESIGN [ICE 4004]

TIME: 3 HOURS MAX. MARKS: 50

Instructions to candidates :*Answer ALL questions and missing data may be suitably assumed.*

1A. Illustrate the twin tub process of CMOS fabrication.

1B. How is SOI technology advantageous over the conventional fabrication technologies?

1C. Determine the pull-up to pull-down ratio for an nMOS inverter driven by another nMOS inverter.

(4+2+4)

2A. Consider nFET chain as shown in Figure Q2A, representing a portion of NAND3 gate. The output capacitance has a value of $C_{out} = 130\ fF$, while the internal values are $C_1 = 36\ fF$ *and* $C_2 = 36\ fF$. The transistors are identical with $\beta_n = 2\ mA/V^2$ in a process where $V_{DD} = 3.3\ V$ *and* $V_{Tn} = 0.7\ V$.

(a) Find the discharge time constant for $C_{out} = 130\ fF$.

(b) Find the time constant if C_1 and C_2 are ignored. What is the percentage error introduced if the internal capacitors are not included?

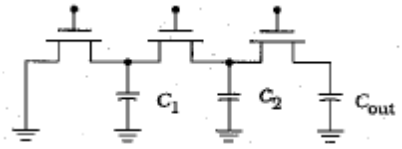

Figure Q2A

2B. A CMOS logic gate that implements the function $f = \overline{x.(y+z)+x.w}$ is needed in a control network. Design the logic circuit by specifying the β_n and β_p values of FETs in the worst case condition.

2C. Sketch stick diagram of a 2-input Ex-OR gate implemented using CMOS logic and estimate the cell width and height in terms of 'λ'.

(3+3+4)

3A. Calculate the delay in the multistage logic network shown in Figure Q3A.

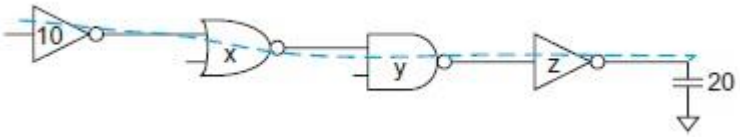

Figure Q3A

3B. Draw the transistor level diagram of a NOR based SR flip flop.

3C. Differentiate between full-custom and semi-custom design.

(2+5+3)

4A. Explain the simple programmable logic devices.

4B. What is the size of the smallest ROM that is needed to implement the following?
(a) An 8-to-3 priority encoder
(b) An 8-to-1 multiplexer
(c) An 8-bit full adder

4C. Implement the function $F = A'B + AB' + AC' + A'C$ using FPGA which has MUX based CLBs. What is the size of the smallest multiplexer needed, assuming inputs and their complements are available?

(4+3+3)

5A. Differentiate between MPGA and FPGA.

5B. Explain different types of faults that need to be tested during circuit design.

5C. What is the importance of packaging in designing an Integrated Circuit (IC)? What are the IC characteristics that affect packaging process?

(2+4+4)

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