Question Paper

Exam Date & Time: 02-Dec-2019 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
END SEMESTER THEORY EXAMINATION - NOVEMBER/ DECEMBER 2019
II SEMESTER B.Sc.(Applied Sciences)in Engg.
Computer Organization and Architecture [ICS 122]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) Perform the following: (6)

A) i) Represent the hexadecimal number C492 in 16 bit and 32-bit binary. ii) Represent -12 in sign and magnitude and 2's complement representations. iii) Add +6 to +3 and Subtract -3 from -6 using 4-bit 2's complement arithmetic. Indicate whether overflow occurs or not in each case.

B) Registers R4 and R5 contain the decimal numbers 4000 and 6000 respectively, before each of the following addressing modes is used to access a memory operand. What is the effective address (EA) in each case? (4)
i) 15(R4)
ii) (R4, R5)
iii) 30(R4, R5)
iv) (R5)

C) Write the flow chart of Booth's algorithm for signed multiplication and explain. Using this algorithm multiply -4 (multiplicand) by +10 (multiplier). Write all the steps showing the intermediate values in the registers. (10)

2) (5)

A) Draw the block diagram of a computer with its essential components, showing the connection between processor and memory. List the steps needed to execute the instruction

Load R2, LOC

which loads the contents of memory location LOC into the register R2, in terms of transfers between the components shown in the block diagram and some simple control commands. Assume that the address of the memory location containing this instruction is initially in register PC.

B) Write and explain the micro operations for interrupt cycle, by making use of data flow diagram and sequence of events. (5)

C) Explain the functioning of the microprogrammed control unit with a neat block diagram. (10)

3) (5)

	A)	Explain the following with respect to memory systems: i) Memory access time ii) Memory cycle time iii) EEPROM iv) Cache memory v) Virtual memory	
	B)	A computer system has 32K words of main memory and a set associative cache. The block size is 16 words and the tag field of the main memory address is 5 bit wide. If the same cache were direct mapped, the main memory will have 3-bit tag field. How many words are there in the cache? How many blocks are there in a cache set?	(5)
	C)	With a neat diagram, explain how data is organized and accessed in a magnetic disk.	(10)
4)		Write the steps of restoring division method for signed numbers. Divide 4 by -3 using this method. Clearly indicate all the steps.	(10)
	A)		
	B)	What do you mean by normalized floating point number? How is it used in 32-bit floating point representation? Represent +25.625 in 32-bit floating point format.	(5)
	C)	Explain Direct and Indirect methods of microinstruction encoding.	(5)
5)		Explain how the I/O devices are accessed by the processor	(10)
	A)		
	B)	Explain clearly the following with respect to cache: i) Write through and write back policy ii) Hit, miss and hit ratio iii) Why replacement algorithms are neaded?	(6)
	C)	Write a note on static RAM.	(4)
6)		Explain the synchronous data transfer over a bus with timing diagram for one block of data transfer per one bus cycle.	(10)
	A)		
	B)	Explain how multiple interrupts are handled in a computer system?	(5)
	C)	Write a note on cache coherence	(5)
7)		What is instruction hazard? Explain with respect to unconditional and conditional branches.	(10)
	A)		
	B)	Explain the concept of pipelined execution	(5)
	C)	Explain two stage machine algorithm for dynamic branch prediction.	(5)
8)		Explain floating point multiplication with an example.	(10)
	A)		
	B)	What are the advantages of Flash drives.	(5)
	C)	Explain UMA and NUMA multiprocessor systems.	(5)

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