# Question Paper

Exam Date & Time: 14-Nov-2019 (02:00 PM - 05:00 PM)

## MANIPAL ACADEMY OF HIGHER EDUCATION

**INTERNATIONAL CENTRE FOR APPLIED SCIENCES**
**END SEMESTER THEORY EXAMINATIONS**
**NOVEMBER2019**
**III SEMESTER B.sc. (Applied Sciences) in Engg.**
**ANALOG ELECTRONIC CIRCUITS [IEC 231]**

**Marks: 100** **Duration: 180 mins.**

**Answer 5 out of 8 questions.**
**Missing data may be suitably assumed.**

1) A) Draw and explain the circuit diagram of common base configuration using NPN transistor. Plot the input and output characteristics. Indicate cut-off, saturation and active regions. (5)

B) The dc common base current gain for a certain transistor is, $\alpha_{dc} = 0.998$ Determine the emitter current $I_E$ if the base current is $I_B$=40$\mu$A . Assume that the reverse saturation current, $I_{CBO}$=2$\mu$A Also determine $I_{CEO}$. (5)

C) Draw the small signal equivalent of the CE amplifier shown in fig. Q1C. Obtain expressions for $g_m$ ,$r_e$ . and output resistance of the amplifier from the model. (5)

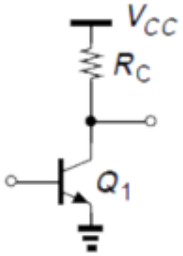
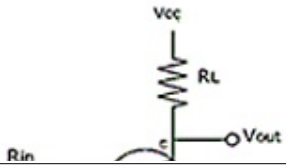



**Fig. Q1C**

D) For the transistor (Silicon) circuit shown in fig. Q1D, $R_{in=}$ 100K$\Omega$, $R_L$=820$\Omega$ and $V_{CC}$=10V Assume $V_{BE}$, sat=0.8V and $V_{CE}$, sat=0.2V. Find the minimum base and collector current required in order to keep the transistor in saturation. Neglect $I_{CBO}$. Explain briefly the working of the circuit and draw the output waveform. (5)



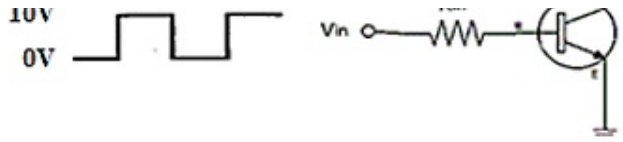
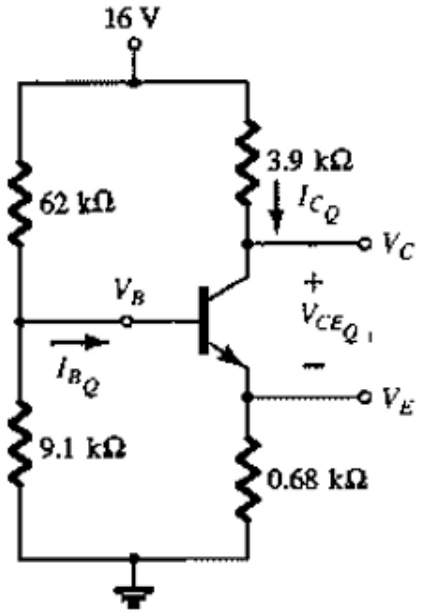



**Fig. Q1D**

2) A) Determine $I_B$, $I_C$, $I_E$, $V_{CE}$, $V_B$, $V_C$ and $V_E$ for the voltage divider configuration shown in Fig Q2A given that β=80. Assume $V_{BE}$=0.7V. What is the region of operation? Neglect $I_{CO}$. (10)




**FigQ2A**

B) Draw the circuit diagram of RC coupled amplifier with feedback using NPN transistor. Mention the function of each component. Explain the working at low, medium and high frequencies. (5)

C) Plot the frequency response of RC coupled amplifier with and without feedback. Indicate the salient features on the plot. In a 3-stage RC coupled amplifier, if the individual stage voltage gains are:$A_1$=50dB, $A_2$=0dB and $A_3$=10dB respectively, find the output voltage at each stage and overall gain in decibels if the input voltage applied is Vi=10sin(2$\pi ft$) millivolts. (5)

3) (5)

A)

For the circuit in **Fig. Q3A**, $\mu_n C_{ox}$ = 100 μA/V$^2$ and $V_{TH} = 0.4V$. Calculate

i) Drain current.

ii) If the gate voltage increases by 20 mV, what is the change in the drain voltage?

iii) What choice of $R_D$ places the transistor at the edge of the triode region with value of $I_D$ as in part i)?

iv) Determine the value of $W/L$ that places $M_1$ at the edge of saturation with $V_{GS}$ as in part i).

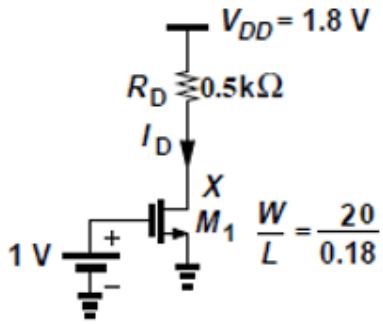



**Fig Q3A**

B) Calculate the maximum allowable gate voltage in **Fig. Q3B**, if $M_1$ must remain saturated. Assume $\mu_n C_{ox}$ = 100 µA/V² and $V_{TH} = 0.4V$ (5)

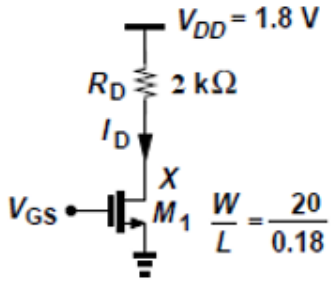



**Fig Q3B**

C) (5)

If λ= 0.1 / V, $\mu_n C_{ox}$ = 100 µA/V², $V_{TH}$=0.4V and $^{W}/_{L} = {}^{10}/_{0.18}$, construct the small-signal model of the circuit shown in **Fig. Q3C.** Compute $V_{DS}$ $g_m$ and $r_o$

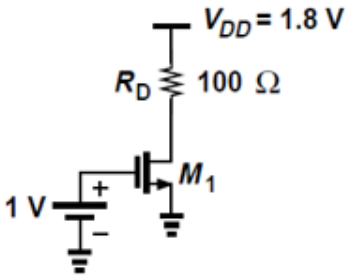


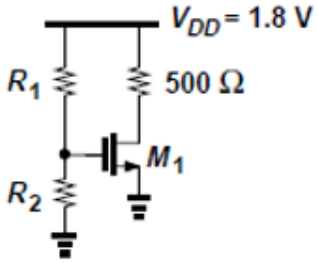

**Fig Q3C**

D) (5)

An NMOS device with $\lambda = {}^{0.1}/_{V}$ must provide a gain of 25 with $V_{DS} = 1$ V. Determine the required value of ${}^{W}/_{L}$, if $I_D = 1$ mA and $\mu_n C_{ox} = 100$ µA/V²

4) (5)

A) Design a circuit of **Fig. Q4A** for a drain current of 1 mA. If ${}^{W}/_{L} = {}^{10}/_{0.18}$, $\mu_n C_{ox} =$ 100 µA/V², $V_{TH} = 0.4V$. Compute R1 and R2 such that the input impedance is at least 50 k.Ω




**FigQ4A**

B) (5)

If ${}^{W}/_{L} = {}^{20}/_{0.18}$, $\mu_p C_{ox} = 200$ µA/V² and $\lambda = 0$, determine $V_{GS}$, $V_{DS}$ and $I_D$ for the circuit shown in **Fig. Q4B**. Draw the small signal model.

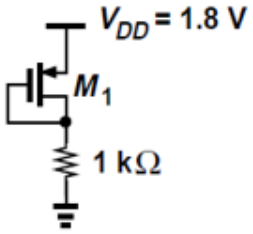



**Fig Q4B**

C) (5)

The CS stage of **Fig. Q4C** must provide a voltage gain of 10 with a bias current of 1 mA. Assume $\lambda_1 = {}^{0.2}/_{V}$, and $\lambda_2 = {}^{0.25}/_{V}$, $\mu_n C_{ox} = 100$ µA/V², $\mu_p C_{ox} = 50$ µA/V² $V_{TH}$=0.4V.

(a) Compute the required value of $({}^{W}/_{L})1$.

(b) If $({}^{W}/_{L})2 = {}^{10}/_{0.18}$, calculate the required value of $V_b$.

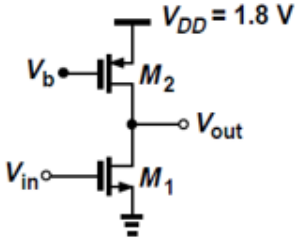



**Fig Q4C**

D) (5)

In the circuit of **Fig. Q4D**, $M_1$ and $M_2$ have lengths equal to 0.2 µm, $\mu_n C_{ox} = 100$ µA/V² $V_{TH} = 0.4V$ and $\lambda = {}^{0.2}/_{V}$. Determine $W_1$ and $W_2$ such that $I_{x1} = 2I_{x1} = 2$ mA. Assume $V_{DS1}$

$V_{TH}$ = 0.4V ,and λ = /V. Determine $W_1$ and $W_2$ such that $I_X = 2I_Y = 2$ mA. Assume $V_{DS1}$ = $V_{DS2}$ = $V_B$ = 1V. What is the output resistance of each current source?

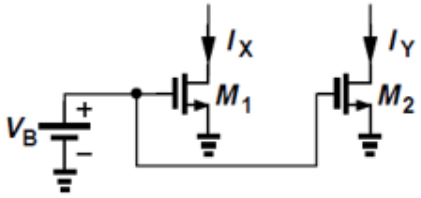



**Fig Q4D**

5) A) State Barkhausen criteria for sustained oscillations. Draw the circuit diagram of Hartley oscillator and explain its working. Write the expression for frequency of oscillations (5)

B) With the help of a circuit diagram, explain the working of transformer coupled Class B push pull power amplifier. Derive an expression for the maximum power efficiency. Mention one drawback of this amplifier. (5)

C) With the help of a block diagram, explain positive feedback. Derive an expression for gain in a positive feedback amplifier. Mention the application of positive feedback. (5)

D) State and explain Millers theorem with an illustration. Explain any one application of this theorem with necessary circuit (5)

6) A) Draw the circuit diagram of High Frequency Model of MOSFET and explain. Write the expressions for the cutoff frequencies on the input and output side of the amplifier. (5)

B) In an RC phase shift oscillator using FET, the value of resistors and capacitors in the feedback circuit are R = 150 KΩ and C = 0.25 Nano Farads. Determine the frequency of oscillation. If the value of $R_D$ =1kΩ and $g_m$ = 2500millimhos, find the gain of the amplifier. (5)

C) With suitable diagrams, explain how power amplifiers are classified based on the operating point. (5)

D) Determine the voltage gain, input and output impedance with feedback for voltage Series feedback having A= -100, $R_i = 10k\Omega$ and $R_o = 20k\Omega$ for feedback of i) β = - 0.1 ii) β = - 0.5 (5)

7) A) Draw the block schematic of i) Voltage shunt ii) Current series feedback amplifiers. What is the effect of series and shunt feedback on the input and output resistance of an amplifier? (5)

B) Draw the circuit diagram of a crystal oscillator and explain the working. Mention any two advantages of Crystal oscillators. (5)

C) Explain the construction, working and characteristics of MOSFET. Sketch output and transfer characteristics. (5)

D) With necessary current equation explain Triode and Saturation region in MOSFET. Explain how current varies when width, length is varied with necessary plot. (5)

8) Explain the following: (20)

i) Early effect in BJT

ii) Channel length modulation in MOSFET

iii) Advantages and disadvantages of Positive and Negative feedback

iv) Piezoelectric effect in crystals
**(5X4=20)**

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