Question Paper

Exam Date & Time: 25-Nov-2019 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
END SEMESTER THEORY EXAMINATIONS
NOVEMBER-2019
III SEMESTER B.Sc. (Applied Sciences) in Engg.
ANALOG AND DIGITAL SYSTEM DESIGN [IMET 234]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data may be suitably assumed.

1)	A)	Minimize the following output function using K-map. $F(X_1, X_2, X_3, X_4) = \Sigma$ m (1, 3, 5, 7, 8, 9, 12, 13) + d(14, 15).	(10)
	B)	Differentiate between combinational and sequential circuits. Draw the block diagram for asynchronous sequential circuit and explain briefly.	(10)
2)	A)	**Convert** (i) T flip-flop into JK flip-flop. (ii) JK flip-flop to SR flip-flop. Explain with truth table and excitation table neatly	(10)
	B)	Draw the block diagram of 4-bit Dual slope ADC.	(10)
3)	A)	Explain the working of a 4 bit R/2R ladder type DAC for the input combinations of 1000,0100, 0010 and 0001 with the help of appropriate circuit diagrams.	(10)
	B)	Explain the working of a D Flip-flop with neat circuit diagram, truth table and also derive the output equation using K-map.	(10)
4)	A)	Design a MOD - 7 asynchronous counter using JK Flip flops.	(10)
	B)	Explain the working of a Johnson counter with neat logic diagram, timing diagram and the count table.	(10)
5)	A)	Implement the following Boolean function using an 8:1 multiplexer. $F(A,B,C,D) = A\overline{B} + BD + \overline{B}\,\overline{C}\,\overline{D}$	(10)
	B)	Design astable multivibrator using 555 Timer for generating a train of pulses of 1.45 KHz and a duty cycle of 56%. Assume C = 0.47µF. Design a monostable multivibrator using 555 timer to produce a pulse width	(10)

of 100ms. Calculate the value of R by assuming the values of C=0.47µF.

6) Convert the following: (10)

A) 42510 = ----------(8)
529.4610 = _____ (2)
ABC.EF16 =_____(10)
42510 =_____(8)
1000.39062510 =_____(16)

B) With a neat logic diagram, explain the working of a SISO shift register. (10)

7) With a neat circuit diagram, explain the working of 2 bit binary adder. (10)

A)

B) Define a decoder. Explain the logic diagram of a 2 to 4 decoder with enable (E) input and a truth table. (10)

8) Explain the working of a synchronous Decade Counter. (10)

A)

B) Describe how an Adder-Subtractor can be created using an Adder circuit and a Subtractor circuit. Use the 741 Op-amp. (10)

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