Question Paper

Exam Date & Time: 28-Dec-2019 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
END SEMESTER THEORY EXAMINATIONS NOVEMBER 2019
III SEMESTER B.sc. (Applied Sciences) in Engg.
SWITCHING CIRCUITS AND LOGIC DESIGN [ICS 232]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) Simplify the following expressions using algebraic manipulation. (12)
i) F(A, B, C, D) = ∑m (3, 7, 9, 12, 13, 14, 15)
ii) f(a, b, c, d, e)=a'c'e'+a'c'd'+a'de+ab'c'e
iii) F(A, B, C,D)=(A'+C'+D')(B'+C'+D)(A+B'+C')
iv) F(A, B, C)=∏M (0, 1, 5)
(4X3=12)

B) i) Derive the minimum cost SOP expression for the following function using K-map and implement using only NOR gates. Write all prime implicants and Essential prime implicants. (8)
F(a, b, c, d)=∑m(0, 1, 2, 5, 7, 8, 10, 12, 14, 15)
ii) Find the minimum cost SOP and POS expression for the following function using K-map.
F(w, x, y, z)=∑m(0, 1, 3, 4, 7, 11, 13, 15) + d(9, 12, 14)
(5+3=8)

2) A) A circuit with two outputs has to implement the following functions (10)
f(x1, x2, x3, x4)=∑m(0, 2, 4, 6, 7, 9) + d(10,11)
g(x1, x2, x3, x4)=∑m(2, 4, 9, 10, 15) + d(0, 13, 14)
Implement it and compare its cost with combined costs of two SOP implementations that implement f and g separately. Assume that the input variables are available in both complemented and complemented forms.

B) i) Perform 2's complement addition for the following : (10)
a) (+5) + (+2) b) (-5) + (+2) c) (+5) + (-2) d) (-5) + (-2)
ii) Design and write the behavioral Verilog code for 4-bit adder/subtractor unit.
(4+6=10)

3) A) i) Design a single-digit BCD adder. (10)
ii) Design and write Verilog code to convert BCD to excess-3 code using a four-bit adder.
(3+7=10)

B) Design a BCD to 2421 code converter using 8:1 MUXes. Write Verilog code to implement this. (10)

4) A) i) Write behavioral Verilog code to convert an N bit binary number into equivalent gray code. Use for loop. (9)
ii) write the truth table and circuit diagram for 4-to-1 Multiplexer.
iii) write the truth table and circuit diagram for three-input majority function using 4-to-1 multiplexer.
(3X3=9)

B) i) Write the truth table for 3-to-8 decoder and design 3-to-8 decoder using two 2-to-4 decoders. (11)
ii) Design and Write Verilog code to implement f (A, B, C) = Σm (0, 2, 3, 4, 5, 7) using 3 to 8 binary decoder and an OR gate. Use case statement.
(5+6=11)

5) A) i) Write the truth table for 4-to-2 priority encoder with active high enable and active low output. (11)
ii) write Verilog code for 8:1 multiplexer using two 2-to-4 decoders and external gates. Implement the 2-to-4 decoder module using for loop.
(3+8=11)

B) i) Design a 4-bit comparator circuit using full adders. The inputs to the comparator are A=a3a2a1a0 and B=b3b2b1b0. The output is AeqB, which is high when A=b and low when A!=B. (9)
ii) A combinational circuit building block receives an 8 bit input A7-0, and produces a 3 bit output Y2-0 and one 1 bit output Z. Y indicates the most significant line number of the input that is TRUE. Z should be TRUE if there are one or more TRUE bits on the input. What is this building block? Draw the block diagram and the truth table.
(3+6=9)

6) A) i) Draw the logic diagram of D flip flop. Write its characteristic table, characteristic equation, and excitation table. (12)
ii) With neat diagram explain the working of D type positive edge triggered Flip-Flop.
(6+6=12)

B) The logic diagram of a sequential circuit is given in Figure Q6.B. Derive the state table and state diagram of the circuit. (8)

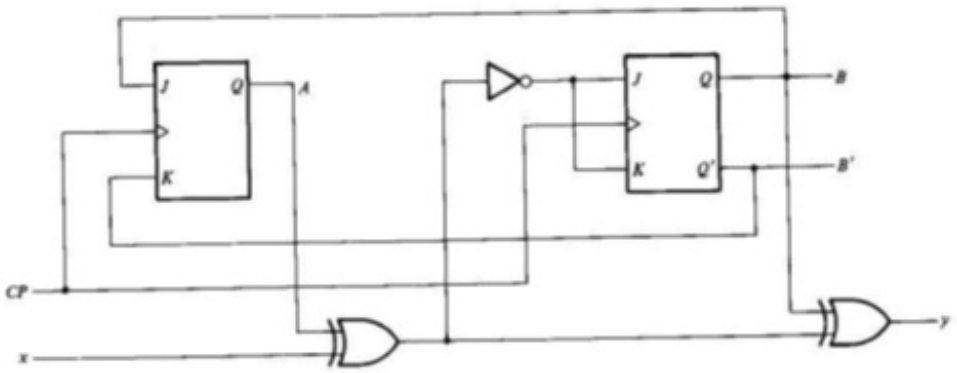

Figure Q6.B

7) A) Design a counter with the following repeated nonbinary sequence: 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops. Treat the unused states as a don't-care (10)

conditions.

B) i. Design a 4-bit bi-directional shift register for the following operations using D flip flops and MUXs. (10)

Shift	Load	Operation
0	0	No change
0	1	Load parallel data
1	d	Shift right

ii. Design and write the Verilog code for 4-bit asynchronous up counter using T Flip-Flop.
(4+6=10)

8) Explain the following with a neat diagram for each. (12)
A) i) NMOS realization of a NAND gate.
ii) NMOS realization of a NOR gate.
iii) CMOS realization of a NAND gate.
iv) CMOS realization of a NOR gate.
(4X3=12)

B) i) Discuss PLA with a neat logic diagram. (8)
ii) Define a tri-state buffer. Write its truth table.
(6+2=8)

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