Question Paper

Exam Date & Time: 18-Nov-2019 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
END SEMESTER THEORY EXAMINATIONS NOVEMBER 2019
III SEMESTER B.sc. (Applied Sciences) in Engg.
SWITCHING CIRCUITS AND LOGIC DESIGN [ICS 232 - S2]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

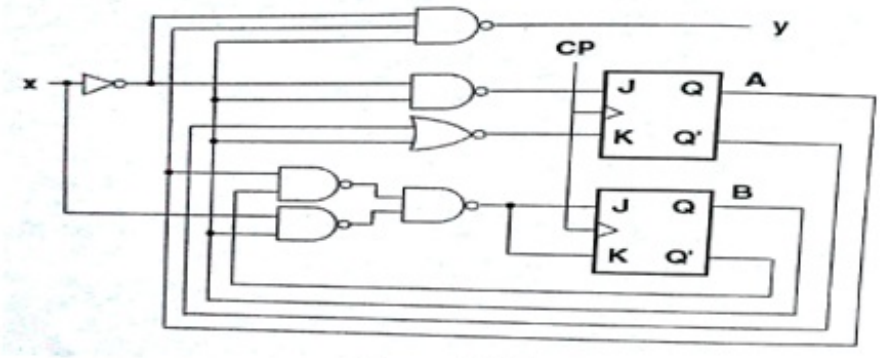
1) A) Simplify the following expressions using algebraic manipulation. (12)
i) F(x1, x2, x3)=x1x3+x1x2'+x1'x2x3+x1'x2'x3'
ii) F=(X+Y'+XY)(X+Y')(X'Y)
iii) F=AB+(AC)'+AB'C(AB+C)
iv) F=(A+B+C)(A'+B+C)(A'+B+C')(A+B'+C)
(4X3=12)

B) i) Find the minimum cost SOP expression for the following function using K-map and implement using only NOR gates. (8)
F(a, b, c, d)=∑m(0, 1, 4, 8, 9, 10, 12, 13)
ii) Derive the minimum cost SOP expression for the following function using K-map and implement using only NAND gates. Write all prime implicants and Essential prime implicants.
F(w, x, y, z)=∏M(2, 3, 6, 8, 9, 11, 12, 13)
(3+5=8)

2) A) A circuit with two outputs has to implement the following functions (10)
F1(A, B, C, D) = ∑m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15).
F2(A, B, C, D)=∑m(6, 7, 8, 9, 13, 14, 15)
Implement it and compare its cost with combined costs of two SOP implementations that implement F1 and F2 separately. Assume that the input variables are available in both complemented and complemented forms.

B) i) Perform 2's complement subtraction for the following : (10)
a) (+5) - (+2) b) (-5) - (+2) c) (+5) - (-2) d) (-5) - (-2)
ii) Write the two cases where correction has to be made during the addition of two single digit BCD. Give examples. Design single digit BCD adder by deriving the expression for the above correction.
(4+6=10)

3) A) i) Design a Four-bit adder/subtractor unit. (10)
ii) Design a 3-bit Arithmetic comparison circuit. Using logic gates derive the expressions for A=B, A< B, and A>B, where A and B are two three-bit numbers. Write Verilog code for the same.
(3+7=10)

	B)	Design a binary to gray code converter using 8:1 MUXes. Write Verilog code to implement this.	(10)
4)	A)	i) Write behavioral Verilog code to convert an N bit gray code into the binary equivalent. Use for loop. ii) Design 4-to-1 multiplexer using 2-to-1 multiplexers. iii) Write the truth table and circuit diagram for three-input XOR function using 4-to-1 multiplexer. **(3X3=9)**	(9)
	B)	i) Design 4-to-16 decoder using two 3-to-8 decoders. ii) A combinational circuit is specified by the following three Functions. F1= X'Y'Z' + XZ, F2=XY'Z' + X'Y, F3=X'Y'Z + XY Design the circuit with a decoder and external gates. Write Verilog code to implement 3 to 8 binary decoder using if then else statement. Use this submodule to implement the above circuit. **(3+8=11)**	(11)
5)	A)	i) Design a 4:16 decoder using four 2:4 decoders and other necessary gates. ii) Design a 3-bit binary to gray code converter using a decoder and other necessary gates. Write the truth table of the code converter and the decoder used in your design. **(4+6=10)**	(10)
	B)	Derive the expressions for 8:3 priority encoder keeping LSB as the highest priority. Write a Verilog code for implementing the same.	(10)
6)	A)	i) Draw the logic diagram of T flip flop. Write its characteristic table, characteristic equation, and excitation table. ii) Using RS Flip-Flop draw the logic diagram of a Master-Slave Flip-Flop. With the help of a sample waveform explain its working. **(6+6=12)**	(12)
	B)	Derive the state table and state diagram of the sequential circuit is given in Figure Q6.B. Where x is an input, and y is an output.  Figure Q6.B	(8)
7)		Design a synchronous BCD down counter using T Flip-Flops.	(10)
	A)		
	B)	i. Design a 4-bit bi-directional shift register for the following operations using D flip flops and MUXs.	(10)

S1	S2	Operation
0	0	No change
0	1	Complement the 4 outputs
1	0	Clear register to 0
1	1	Load parallel data

ii. Design and write the Verilog code for 4-bit Johnson counter using D Flip-Flop.

(4+6=10)

8) Explain the following with a neat diagram for each. (12)

A) i) NMOS realization of a AND gate.
ii) NOT Gate built using NMOS Logic
iii) CMOS realization of a NOT gate.
iv) Multiplexer circuit using Transmission gates

(4X3=12)

B) i) Write the different types of power dissipation in switching circuits. Explain the power dissipation(s) that occurs in NMOS and CMOS circuits. (8)
ii) With neat diagram and explain the application of tristate buffers.

(6+2=8)

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