Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

III SEM B.Tech (BME) DEGREE MAKE UP EXAMINATIONS, DEC/JAN 2019-20.

SUBJECT: ANALOG ELECTRONICS (BME 2151)
(REVISED CREDIT SYSTEM)
Friday, 20th December, 2019: 8.30 AM to 11.30 AM

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer ALL questions.**
2. **Draw labeled diagram wherever necessary**
3. **Assume suitable data, if missing**

1. (A) An NPN Silicon transistor having $\beta = 100$ is in common-emitter configuration, and is biased by fixed bias method. The circuit parameters are $R_B = 530K\Omega$, $R_C = 3K\Omega$, and V_{CC} = 6V. Draw the circuit diagram and determine 5
   (i) the d.c load line
   (ii) the operating point, and
   (iii) the stability factor

   (B) For the circuit drawn for question no.1(A), draw the a.c equivalent circuit and determine the input and output impedances. Assume that the transistor is operated at room temperature, and output resistance of the transistor is infinity. 3

   (C) Draw the circuit diagram of a voltage-series feedback amplifier employing a BJT, and derive expression for de-sensitivity (D). 2

2. (A) Making use of transfer curve and bias line determine the operating point of the Enhancement MOSFET circuit shown in figure 2(A). 5

   (B) In an UJT relaxation oscillator, the UJT and the circuit parameters are $R_{BB} = 8K\Omega$, $\eta = 0.7$, $R_1 = 0.2K\Omega$, $R_E = 40K\Omega$, $C_E = 0.12\mu F$, V_V = 2V, I_V = 10mA, $I_p = 10\mu A$, V_D = 0.7V, and V_{BB} = +12V. 3
   (i) Determine value of RB_1 and RB_2 required, when I_E = 0mA
   (ii) Calculate the value of V_E required to turn on the UJT
   (iii) Find the approximate frequency of oscillation

   (C) Determine the voltage gain and input impedance of the voltage-series feedback amplifier shown in figure 2(C). 2

3. (A) An n-channel JFET in common-source configuration is biased using voltage-divider biasing network with the source terminal resistor bypassed by a capacitor. 5
   (a) Draw the circuit diagram
   (b) Draw the small signal model, and
   (c) Prove that $Z_i = R1||R2$ and $A_V = -g_m (r_d ||R_D)$

   (B) For a JFET in fixed bias network, prove that the input impedance is $R_G(\Omega)$. 3

   (C) How does the conduction channel get pinched-off in a JFET? 2

4. (A) For the FET circuit shown in figure no. 4(A), chose appropriate values of R_D and R_S so as to establish a gain of 8 at $V_{GSQ} = \frac{1}{4}V_P$. 5

(B) If a JFET in a fixed bias network has V_{GG} = -1V, $R_G = 2M\Omega$, V_{DD} = +12V, and $R_D = 2K\Omega$. And from the data sheet I_{DSS} = 8mA and V_P = -5V. Determine V_{GSQ} and I_{DQ}. 3

(C) Draw typical drain and transfer characteristics of a depletion type MOSFET. 2

5. (A) For a Class-C power amplifier prove that the Power output is $\frac{V_{CC}^2}{2r_C}$ and the efficiency is 95%. 5

(B) Compute the value of R2 required to provide trickle current for distortion free output in the push-pull amplifier shown in figure no. 5(B). Assume V_{BE} = 0.7V for each transistor. 3

(C) Design a current-series feedback amplifier to have an overall trans-conductance gain of -1mA/V, a voltage gain of -4, and a de-sensitivity of 50. Make use of a NPN type BJT having h_{fe} = 150, and assume a signal source with a resistance of 1KΩ. Draw the labelled circuit diagram of the designed amplifier. 2

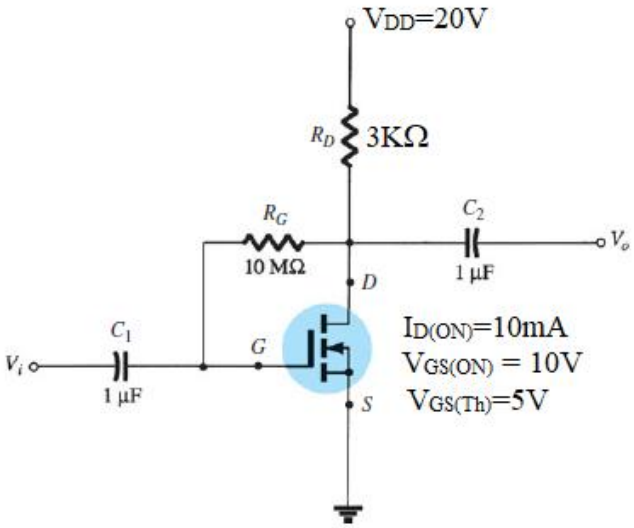

Fig. 2(A)

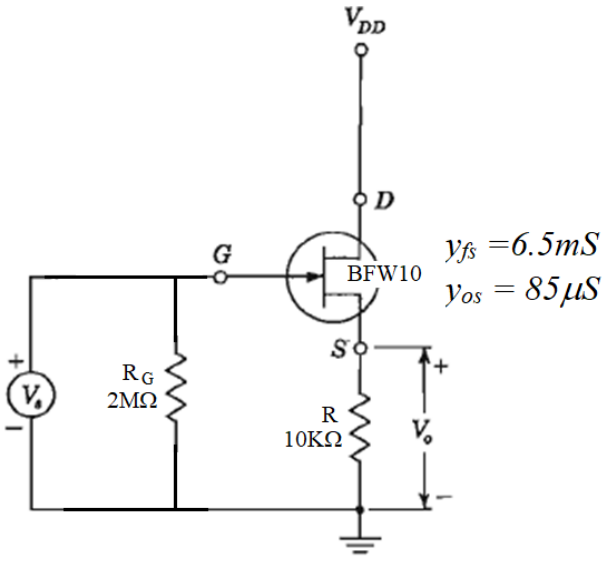

Fig. 2(C)

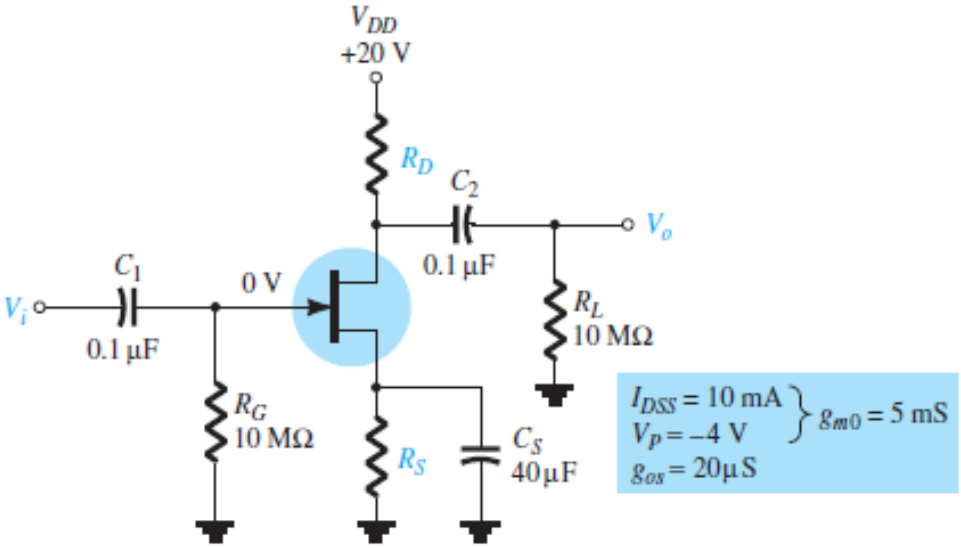
V_{DD}
+20 V
R_D
C_2
V_o
0.1 μF
C_1
0 V
V_i
0.1 μF
R_L
10 MΩ
R_G
10 MΩ
R_S
C_S
40 μF
I_{DSS} = 10 mA
V_P = −4 V
g_{os} = 20 μS
g_{m0} = 5 mS

Fig. 4(A)

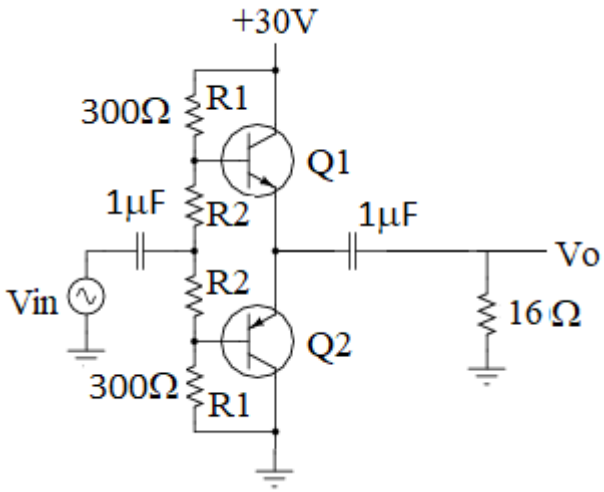
+30V
300Ω
R1
Q1
1μF
R2
1μF
Vo
Vin
R2
16 Ω
Q2
300Ω
R1

Fig. 5(B)