Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

DEGREE EXAMINATIONS [November 2018]

SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]

REVISED CREDIT SYSTEM
(22-11-2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- All the inputs are available only in ***true*** form.

1A. i. Prove the validity of the following expression using algebraic manipulation. Justify your answer. **(2+2)M**

x1'x3+x1x2x3'+x1'x2+x1x2'=x2'x3+x1x3'+x2x3'+x1'x2x3

ii. Simplify the following function using K map. Write all the essential prime implicants and find the minimum cost POS expression.

$F(a,b,c,d) = \sum m(1,3,4,5,7,8,9,11,12,15)$

1B. Find the minimum cost SOP expression for the following function. Design the circuit using only NAND gates from the minimum cost SOP expression obtained. **3M**

$F(a,b,c,d) = \pi M(1,3,5,8,9,11,15) + d(2,13)$

1C. Use functional decomposition to find the best implementation for the following function **3M**

$F(a,b,c,d,e) = \sum(1,2,5,7,9,10,13,15,18,19,25,26,29,31)$

2A. Design and write the Verilog code for a single digit BCD adder. **4M**

2B. Design a circuit using only basic gates, which takes a 4 bit signed number in its 2's complement representation as input and will find the 1's complement representation for the same signed number as output. [Sample input: 1001 output: 1000]. The input '-8' which does not have a 1's complement representation in 4 bit can be assumed to give a don't care as output. **4M**

2C. Design a circuit which takes two 4 bit signed numbers X and Y as input and gives the output '1' if the result of the operation 'X-Y' is positive(>=0). The output is '0'otherwise. **2M**

3A. A combinational circuit receives two single-bit inputs a, b and produces two-bit output Y=F1+F2+F3.The boolean functions F1, F2 and F3 are implemented using a decoder as given below. Design a minimal circuit for Y using only one decoder, two 4:1 multiplexers, three OR gates and one inverter. **4M**

$F1(a,b)=\sum m(1,3)$ $F2(a,b)=\sum m(0,2,3)$ $F3(a,b)=\sum m(1,2,3)$.

Write the behavioral Verilog code to implement the same.

3B. i. Design a 16:1 multiplexer using only 4:1 multiplexers. **(1+2)M**

ii. Use Shannon's expansion to derive a minimal cost implementation for the function F(a,b,c)=a'b'c+abc'+a'bc+ab'c', with a 2:1 multiplexer and other necessary gates.

3C. Write the truth table for an 8 to 3 priority encoder. Provide an output 'Z' to indicate that at least one of the inputs is high. The input with the least subscript number has the highest priority. Write the behavioural Verilog code to implement the same using ***for*** loop. **3M**

4A. Distinguish between blocking and non-blocking assignments. Draw the circuits for the Verilog code segments given in (a) and (b) using D flip-flop(s). **3M**

(a) always @(negedge clock)
begin
f = a & b;
g = f | (c ^ d);
h = ~ g ^ (a | d);
end
	(b) always @(posedge clock)
	begin
	f <= a & b;
	g <= f | (c ^ d);
	h <= ~ g ^ (a | d);
	end

4B. i. Design a JK flip-flop using D flip-flop and other necessary gates. **(3+2)M**

ii. Design D flip-flop using T flip-flop and other necessary gates.

4C. Design a 4 bit Johnson counter. Write the truth table showing the count sequences and find the AND gate expressions required to generate 8 timing signals. **2M**

5A. With a neat diagram explain the working of CMOS realization of a NOT gate. **3M**

5B. i. Draw the customary schematic for the PLA which implements the function $F(a,b,c)=\Sigma m(0,2,3,7)$ and $G(a,b,c)=\Pi M(0,1,4,6)$. **(2+2)M**

ii. Write the different types of power dissipation in Transistor circuits. Explain the power dissipation(s) that occurs in NMOS and CMOS circuits.

5C. What is a tristate buffer? With neat diagram and explain the different types of tristate buffers. **3M**