Exam Date & Time: 19-Nov-2019 (09:00 AM - 12:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH (COMPUTER AND COMMUNICATION ENGINEERING)
END SEMESTER EXAMINATIONS, NOV 2019
DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2171]

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Instructions to Candidates: Answer ALL questions. Missing data may be suitably assumed.

1) A) Design a self-correcting synchronous counter using T - flip flops and minimum number of external gates to count the sequence $1 \rightarrow 4 \rightarrow 6 \rightarrow 3 \rightarrow 2 \rightarrow 1$ when control input Y=0 and count the sequence $1 \rightarrow 5 \rightarrow 7 \rightarrow 6 \rightarrow 4 \rightarrow 1$ when control input Y=1. The undefined count should restart the counter from count 1 during the next clock. (5)

B) Given M = - $9_{(10)}$ and Q = - $5_{(10)}$, multiply using Booth's Algorithm indicating all the steps. (3)

C) Design a 4:2 priority encoder using basic logic gates. (2)

2) A) Design a hardwired control unit for 4x4 Booth's multiplier. (5)

B) What is race around condition? How is it overcome in T – flip flop using Master-Slave configuration? (3)

C) Design SR – flip flop using D – flip flop and external gates. (2)

3) A) Design a sequence detector with one input Y and one output Z. The output Z is HIGH whenever the sequence "1101" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using JK- flip flops and minimum number of external gates. (5)

B) A Computer system has a 32K of main memory and 4K of cache memory. The cache block size is 8 words. Calculate the tag field width for fully associative mapping, direct mapping and 4-way set associative mapping schemes. Also, write the limitation of fully associative mapping and direct mapping schemes. (3)

C) Differentiate Carry Look-ahead Adder, Carry Save Adder and Carry Propagation Adder with an example (2)

4) Design a code converter to convert a decimal digit represented in 5 2 1 1(self-complementing) to a decimal digit represented in excess-3 code, using 74138 ICs and external gates. (5)

A)

B) Using only JK – flip flops, design a MOD 10 counter circuit to generate an output waveform with 50% duty cycle. Using this, generate the sequence 0001111100. (3)

C) Design a 3 – bit universal shift register using D – flip flops and Multiplexers. (2)

5) Using 7493 ICs, 7485ICs and external gates, design a 2 – digit decimal counter which counts from 00 to N ($00 < N < 99$) and repeats. (5)

A)

B) Design a 3-bit magnitude comparator using minimum number of 4:1 and 2:1 multiplexers ONLY. (3)

C) Explain the operation of a Direct Memory Access System. (2)

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