Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKE UP EXAMINATIONS, DECEMBER 2019

ANALOG SYSTEM DESIGN [ELE 2151]

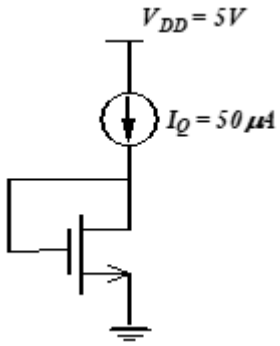
REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 02 JANUARY 2020** **Max. Marks: 50**

Instructions to Candidates:

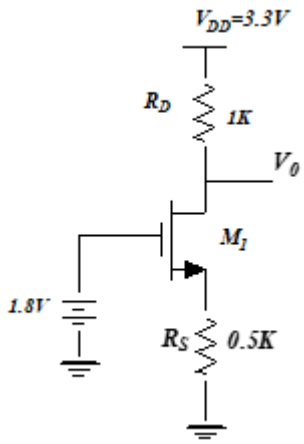
- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Determine V_{GS} and V_{DS} . Assume V_{TH} =1.2V and $\mu_n C_{ox}\left(\frac{W}{L}\right) = 1mA/V^2$



(02)

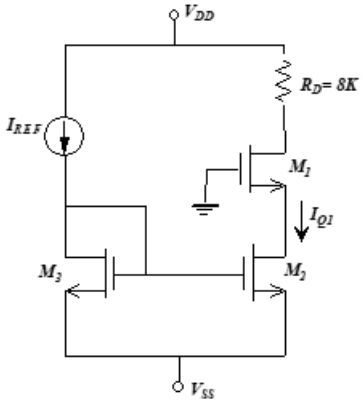
1B. The transistor has $V_T = 1V$ and $\mu_n C_{ox}\left(\frac{W}{L}\right) = 2mA/V^2$. Determine V_{GS}, I_D, V_0.



(03)

1C. Assuming circuit parameters, $I_{REF} = 120\mu A, V_{DD} = 3V$ and $V_{SS} = -3V$, transistor parameters of $V_{TH} = 0.4V, \frac{1}{2}\mu_n C_{0x}\left(\frac{W}{L}\right)_1 = 50\mu A/V^2$, $\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 = 30\mu A/V^2$, $\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 = 60\mu A/V^2$. Determine I_{Q1}, V_{GS1}, V_{GS3} and V_{DS1}.

(05)



2A. Write a note on channel pinch off. ***(02)***

2B. With suitable circuit and small signal model, derive the expression for the gain of common drain MOS Amplifier. ***(03)***

2C. Draw the circuit of an RC coupled Amplifier and state the importance of all the capacitors and resistors. ***(05)***

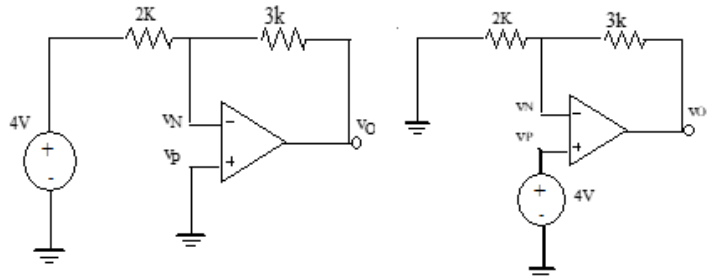
3A. Explain the working of voltage to current converter with grounded load. ***(02)***

3B. Design a single OP-AMP based circuit to get $V_0 = 8V_a - 6V_b - 2V_c$. Assume feedback resistor and noninverting terminal to ground resistor as 12KΩ. ***(03)***

3C. Explain the significance of buffer in instrumentation amplifier and derive the overall gain in the instrumentation amplifier. ***(05)***

4A. Draw the opamp based square wave generator obtain the component values to get a pulse of 2kHz frequency. Assume C=0.01μF and feedback factor β=0.46. ***(02)***

4B. Determine v_P, v_N, v_o for the OPAMP based circuits.



(03)

4C. Design a first order band rejection filter to reject the frequencies in the range 2kHz-5kHz, with a pass band gain of 2. Assume C=0.01μF if required. Sketch the filter circuit diagram. ***(05)***

5A. Draw the circuit of a half wave precision rectifier and explain the working. ***(02)***

5B. Discuss the working of phase locked loop. ***(03)***

5C. Design a 555 timer based circuit to generate a pulse train of 1kHz frequency with 50% duty cycle. What changes are required to obtain 75% duty cycle? Assume C=0.01μF if required. ***(05)***