Exam Date & Time: 19-Nov-2019 (09:00 AM - 12:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH (INFORMATION TECHNOLOGY) END SEMESTER EXAMINATIONS, NOV 2019

DIGITAL SYSTEMS [ICT 2154]

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Instructions to Candidates: Answer ALL questions. Missing data may be suitably assumed

1) A) Design a self-correcting synchronous counter using T - flip flops and minimum number of external gates to count the sequence $1 \rightarrow 4 \rightarrow 6 \rightarrow 3 \rightarrow 2 \rightarrow 1$ when control input Y=0 and count the sequence $1 \rightarrow 5 \rightarrow 7 \rightarrow 6 \rightarrow 4 \rightarrow 1$ when control input Y=1. The undefined count should restart the counter from count 1 during the next clock. (5)

B) Design a 3-bit x 2-bit binary multiplier using Half adder blocks only. (3)

C) Design a 4:2 priority encoder using basic logic gates. (2)

2) A) Simplify the given function 'F' using tabulation method. Implement the simplified expression using NOR gates only. $F(v,w,x,y,z) = \sum m(1,5,9,11,13,20,21,26,27,28,29,30,31) + d(3,17,19)$. (5)

B) What is race around condition? How is it overcome in T – flip flop using Master-Slave configuration? (3)

C) Design SR – flip flop using D – flip flop and external gates. (2)

3) A) Design a sequence detector with one input Y and one output Z using Moore model. The output Z is HIGH whenever the sequence "1101" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using JK- flip flops and minimum number of external gates. (5)

B) Following sets of Boolean functions are to be realized using 3 x 5 x 3 Programmable Logic Arrays (PLA). Draw the logic diagram of the realization in Programmable Logic Device notation and also write the corresponding PLA table. (3)

$F_1(a,b,c) = \sum m(1,3,4,6)$

$F_2(a,b,c) = \sum m(0,2,4,5,7)$

$F_3(a,b,c) = \sum m(1,3,5,6,7)$.

C) Design a 2-bit Carry Look-ahead Adder. (2)

4) Design a code converter to convert a decimal digit represented in 5 2 1 1(self-complementing) to a decimal digit represented in excess-3 code, using 74138 ICs and external gates. (5)

A)

B) Using only JK – flip flops, design a MOD 10 counter circuit to generate an output waveform with 50% duty cycle. Using this, generate the sequence 0001111100. (3)

C) Design a 3 – bit universal shift register using D – flip flops and Multiplexers. (2)

5) Using 7493 ICs, 7485ICs and external gates, design a 2 – digit decimal counter which counts from 00 to N ($00 < N < 99$) and repeats. (5)

A)

B) Design a 3-bit magnitude comparator using minimum number of 4:1 and 2:1 multiplexers ONLY. (3)

C) Using Karnaugh map, determine simplified sum of products and product of sums expressions for the function $F(A,B,C,D,E) = \Pi M(1,3,4,5,11,14,15,16,17,19,20,24,26,28,30)$ (2)

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