MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent institution of MAHE, Manipal)

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)
MAKE UP EXAMINATIONS, DEC 2019
SUBJECT: DIGITAL SYSTEM DESIGN [MTE 2152]
CREDIT SYSTEM
(26 /12 /2019)

1A	Realize the Boolean function $f(W, X, Y, Z) = \sum m(1,3,5,7,8,12,14)$ using i. Basic gates ii. Only NAND gates iii. Only NOR gates	5	CO1
1B	Design a one digit BCD adder using 74LS283.	3	CO2
1C	Draw the flow chart of Digital system design flow.	2	CO4
2A	Realize the Boolean function $f(w, x, y, z) = \sum m(0,1,5,6,7,9,13,14)$ using a) 8 to 1 multiplexer b) 4 to 1 multiplexer with gates at the input c) 4 to 1 multiplexer with 2 to 1 multiplexers at the input.	5	CO2
2B	Define a programming element in an FPGA. Llist the 4 programming elements, mentioning the differences between them.	3	CO4
2C	Demonstrate a 4 to 16 decoder using 2 to 4 decoders.	2	CO2
3A	Design a synchronous 3 bit gray code up counter using D flip flops.	5	CO3
3B	Implement a mod 60 counter using 74LS90.	3	CO3
3C	What is race around condition? Mention the condition and type of flip flop in which it occurs. How can it be avoided?	2	CO3
4A	Design an Asynchronous Mod 8 up counter using JK flip flops. Draw the waveforms at each flipflop to show the entire count.	5	CO3
4B	Draw the state diagram (Mealy m/c) of a sequence detector which has a single input x and a single output z. The output variable z will be high if it detects 1001 and 011 in a continuous data stream.	3	CO3
4C	Draw the logic circuit of a 4 bit Ring Counter with single circulating '1' using IC74194 wired as left shift.	2	CO3
5A	Design a sequence detector (Moore FSM) to detect the sequence 010 in a continuous data input stream. Use D Flip flops.	5	CO3
5B	Write a gate level Verilog code for a 1 bit full adder. Using this as a component write a structural Verilog code for a 4 bit full adder.	3	CO5
5C	Write a behavioural Verilog code for a one bit full adder	2	CO5