MANIPAL ACADEMY of HIGHER EDUCATION
(Deemed to be University under Section 3 of the UGC Act, 1956)

Reg. No.										

DEPARTMENT OF SCIENCES, I/III SEMESTER M.Sc. (PHYSICS)
END SEMESTER EXAMINATIONS, NOVEMBER 2018
SUBJECT: Fundamentals of Electronics [PHY 4107]
(REVISED CREDIT SYSTEM-2017)

Time: 3 Hours Date: 23-11-2019 MAX. MARKS: 50

Note: (i) Answer **ALL** questions

(ii) *Draw diagrams, and write equations wherever necessary*

1. (a) Sketch the logic system for a clocked JK flip flop and give its truth table. (3M)

(b) Use a Karnaugh map to minimize the following standard SOP expression
$\bar{B}\ \bar{C}\ \bar{D}$ + $\bar{A}$ B $\bar{C}$ $\bar{D}$ + A B $\bar{C}$ $\bar{D}$ + $\bar{A}$ $\bar{B}$ C D +A $\bar{B}$ C D + $\bar{A}$ $\bar{B}$ C $\bar{D}$ + $\bar{A}$ B C $\bar{D}$ + A B C $\bar{D}$ +A$\bar{B}$ C $\bar{D}$ (3M)

(c) What is a multiplexer? Explain the basic operation of a four input multiplexer and draw its logic diagram. (4M)

2. (a) Draw the state diagram, flip flop transition table, Karnaugh map for the terminals J_0 and K_0 that is necessary for the design of a three bit Gray code counter. And obtain Boolean expression for J_0 and K_0. (4M)

(b) Draw the four-bit binary ladder. Obtain expressions for the output voltages due to MSB and LSB. (4M)

(c) Draw the circuit diagram of voltage regulator using series transistor and opamp . (2M)

3 (a) Draw the differential amplifier circuit and obtain an expression for the voltage gain in single ended operation. (4M)

(b) Describe how an op-amp can be used as Schmitt triger. (4M)

(c) Explain the concept of virtual ground with referance to op-amp. (2M)

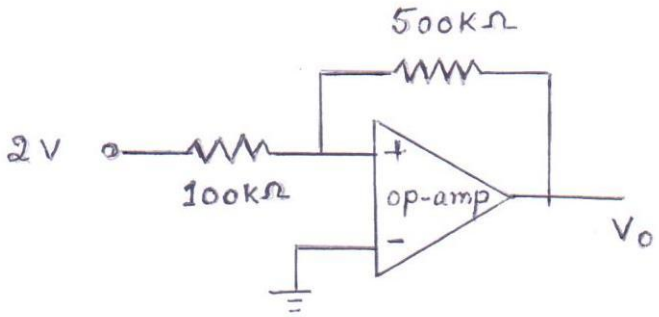
4. (a) Draw the block diagram of 555 timer . Explin how 555 timer can be used for monostastable operation and find the formula for the pulse width.

(5M)

(b) Draw the circuit diagram for the first order low pass filter using op-amp and derive an expression for upper cut off frequency.

(3M)

(c) Find the output voltage V_o in the following circuit.



(2M)

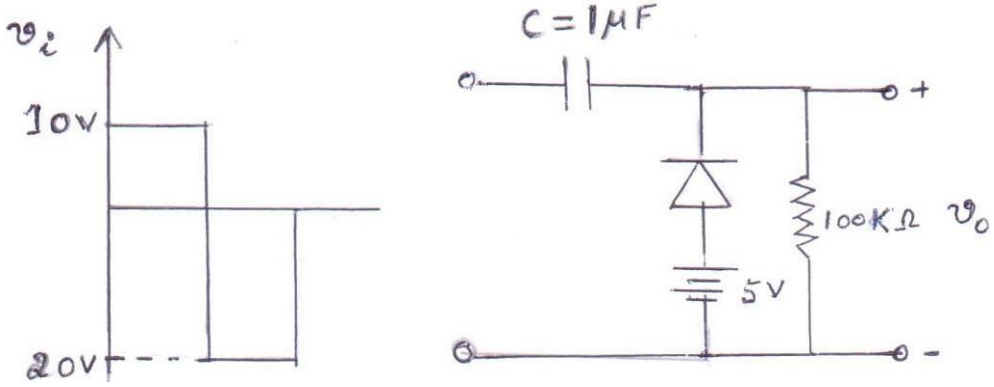
5. (a) Draw ac equivalent circuit for transistor in CE configuration ..Use it to find the input impedane,output impedance and voltage gain of a transistor in CE configuration with voltage divider bias.

(5M)

(b) Discuss the constuction and working of UJT.Draw its equivalent circuit and I-V charecterstics.

(3M)

(c) Determine v_0 for the network given below for the input indicated.



(2M)