Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

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(A constituent unit of MAHE, Manipal)

I SEMESTER M. TECH (POWER ELECTRONICS AND DRIVES)
END SEMESTER EXAMINATIONS, NOVEMBER 2019

EMBEDDED SYSTEM DESIGN [ELE 5171]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: November 19 , 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. i. Describe Dhrystone benchmark with respect to processing power of a processor and hence define the term DMIPS.

ii. Write a technical note on EEMBC. List any four processor benchmarks defined under EEMBC and explain in brief. ***(04)***

1B. i. List the main features and specifications of PIC16F877 microcontroller.

ii. Explain the following PIC16F877 instructions. Illustrate with an example.

a. XORWF f, d

b. BTFSC f, b ***(04)***

1C. 200, '32' bit numbers are available in memory locations starting at 0x00003000. Write an ARM7 ALP to copy these data to successive locations starting at ox00004000 and clear the source memory (data in all source locations should be zero.) ***(02)***

2A. Write ARM7TDMI assembly code for the following 'C' code. Use refgisters R0 to R6 for variables 'a' to 'g' respectively.

```
if (a = = b) && ( c = = d)
   {
      e = 7* (a+b);
      f = - f ;
      g = [g + 9 * (c*d)];
   }
```

(03)

2B. Write an ARM7 subroutine to find the ASCII code for upper and lower nibbles of an '8' bit binary number passed to subroutine through D_7 to D_0 bits of 'R0' register. Return the result through registers 'R1' and 'R2'. (Hint: Add 30H, if the nibble value is less than or equal to 9 and add 37H if the nibble value is between 'A' and 'F'). ***(03)***

2C. Answer the following with respect to ARM7 exceptions

i. Describe the sequence of (step by step) operation in ARM7 when an exception occurs.

ii. Assuming you are writing code for RESET exception handler in supervisor mode, write ARM7 instructions to enable IRQ and FIQ interrupts and to change the mode of operation to user mode. ***(04)***

3A. Describe the salient features of SRAM and DRAM devices. List their relative merits and de merits. Mention the applications of these devices in embedded systems. ***(03)***

3B. With the help of a relevant timing diagram, explain PCI bus protocol for memory read operation to transfer three '8' bit data in the data field. Assume that target device takes three clock cycles to respond to address sent by initiator. No wait cycles are required in case of data '1'. Target requests for two wait (extra) cycles during data '2' and initiator requests for one wait (extra) cycle during data '3'. Explain clearly the role and functions of all the signals involved in the communication. ***(03)***

3C. Write a 'C' program for PIC16f877 microcontroller to configure the MSSP in I2C master mode to transmit data bytes 9AH and 8BH to slave device '1' with address 79H and then (before stop condition is issued) transmit data bytes EEH and FFH to slave device '2' with address 08H at 400kbps baud rate. Assume fosc = 16MHZ. ***(04)***

4A. Describe the protocol used by CAN serial communication bus for data transfer. Explain in detail all the fields involved in the data transfer. ***(03)***

4B. i. If positive and negative reference voltages of ADC in PIC16F877 are '5' V and '0' V respectively, determine the values of ADRESH and ADRESL registers with left justified result format, when an analog voltage input of 4.4V is converted to digital.

ii. Write a 'C' program to convert the analog input applied to RE1 / AN6 pin of PIC16F877 microcontroller and display the result at ports 'B' and 'D'. Use left justified result, conversion time of 24μs, positive and negative reference voltages from RA3 / AN3 and RA2 / AN2 pins. All the remaining pins of ports A and E should be available as analog input pins. Take f_{osc} = 1MHz. ***(04)***

4C. With the help of a relevant diagram, explain the infrared (wireless) communication as per SIR standard using IR encoder /decoder and IR transceiver. ***(03)***

5A. i. Describe the features, working and timeout selection details of watchdog timer in PIC16F877 microcontroller.

ii. With the help of a relevant pseudocode, explain how ATM timeout can be realized using watchdog timer. ***(04)***

5B. With the help of a neat diagram, explain the daisy chain arbitration scheme for interrupt expansion. Compare it with priority arbitration scheme and list the merits and demerits. ***(03)***

5C. Describe the main characteristics of real time systems and hence compare it with non-real time systems. ***(03)***