MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.) END SEMESTER DEGREE EXAMINATIONS, DECEMBER - 2019

SUBJECT: MICROPROCESSORS & MICROCONTROLLERS [ICE 3104]

TIME: 3 HOURS

MAX. MARKS: 50

Instructions to candidates : Answer ALL questions and missing data may be suitably assumed.

- 1A. List the factors that need to be considered while choosing a Microcontroller?
- 1B. What do you mean by assembler directives? Explain any two assembler directives in 8051.
- 1C. Explain the function of the following pins of 8051 microcontroller.i) I/O port pins ii) AD0-AD7 iii) T0,T1 iv) TXD,RXD v) XTAL1,XTAL2

(2+3+5)

- 2A. Write an 8051 program to toggle P1.4 and P1.5 continuously without disturbing the rest of the bits.
- 2B. What is the function of CALL instruction in 8051 Microcontrollers? Explain the different type of CALL instructions available.
- 2C. Consider an array of 10 numbers stored in the internal memory from 30h onwards. Write an ALP to keep the count of the numbers that are greater than, less than and equal to 0Bh.
- 3A. Explain the simplex and duplex mode of data transfers.
- 3B. What do you mean by interrupts? Explain setting of interrupt priority in 8051 Microcontrollers.
- 3C. Explain the format of TMOD register. Generate a square wave of 66% duty cycle. Assume XTAL=11.0592MHz. Use Timer 0 in mode 2.

(2+3+5)

(2+3+5)

(2+3+5)

- 4A. Explain Big Endian and Little Endian memory storage formats in ARM processors.
- 4B. Write the format of current program status register in ARM. Explain how the setting /resetting of different bits controls the ARM functioning.
- 4C. Explain how the stack is accessed in ARM processors. Illustrate full/empty, ascending/descending stack.
- 5A. List any four features of LPC2148 Microcontrollers.
- 5B. Mention any six timer registers in LPC2148 and explain their importance.
- 5C. What is the function of PWMMR and PWMMCR registers? Write the code for LPC2148 to generate a square waveform on P0.4-P0.7, with 50% duty cycle.

(2+3+5)
