Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

V SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DEC 2019

SUBJECT: FPGA Based Digital System Design [MTE 4014]

(01/01/2020)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Data not provided may be suitably assumed
- Graph sheets will be provided

1A.	Discuss the structure of Verilog module and write a Verilog code for 4-bit adder module.	**03**	**CO1**
1B.	Develop a verilog program for the Boolean function f=maxterms{2,3,4} using a) Gate level structural modelling. b) Data flow modelling c) Behavioural Modelling	**04**	**CO1**
1C.	Write a Verilog module for 4:1 MUX using case statements.	**03**	**CO1**
2A.	Realize the boolean function f=maxterms{0,2,3,4,5} using PROM and PLA.	**03**	**CO2**
2B.	Describe the internal structure of XC9500 family.	**04**	**CO2**
2C.	Discuss how an FPGA structure can be used to develop combinational logic of function f=maxterms{1,2,3,4,5,6,7,8,9,10,11,12,13,14}.	**03**	**CO3, CO4**
3A.	Explain stuck at faults and identify the total number of stuck at faults possible for the logic shown in Fig. 3a	**03**	**CO4**

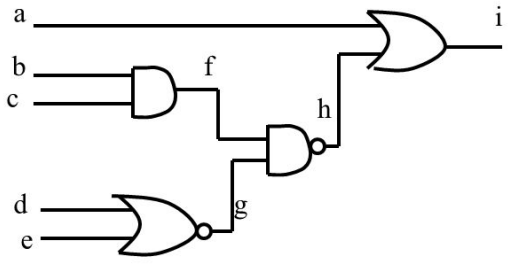

Fig. 3a

3B.	Summarize the internal structure of ALTERA APEX 20K FPGA.	**04**	**CO3**
3C.	Describe the Built in Test Architecture and its necessity in Digital System Design.	**03**	**CO4**
4A.	Write a Verilog HDL program for synchronous RAM module with size of 32 word lines and each word with byte size.	**04**	**CO1**

4B.	State the design flow steps of FPGA and write a simulation testbench for 1:4 DeMux.	**04**	**CO1, CO3**
4C.	Write a Verilog task for RPM to rps speed conversion.	**02**	**CO1**
5A.	Discuss on fault testing of sequential circuits.	**03**	**CO4**
5B.	A synchronous signal function generator with single output is to be designed and developed with FPGA technology having 50MHz rate which meets the following specifications: • Generates a triangular waveform with 50KHz period. • Generates a sawtooth ramp waveform with 0.1MHz period. • Generates a square pulse with ON for 5µsec and OFF for 5µsec. • The function generator has a waveform selector and also is provided for reset option of the function generator waveform. With neat waveforms of function generator develop a Verilog code for this case study of digital function generator application.	**07**	**CO4**