Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, NOVEMBER 2019

EMBEDED PROCESSOR ARCHITECTURE [ELE 4003]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 23 November 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Discuss the different Architectural style and describe the advantages / disadvantages of load-store architecture? ***(05)***

1B. Describe the different data Hazards which is associated with Load /Store architecture. ***(05)***

2A. List the four Bus cycle associated with ARM7TDMI and How it is initiated by processor using nMREQ and SEQ signals. ***(05)***

2B. Write the neat diagram of dataflow model of ARM 9TDMI and explain register to register and register to immediate dataflow. ***(05)***

3A. Explain different operation performed by Register7 of CP15 and write assembly code to flush entire cache in ARM940T ***(04)***

3B. List out the different Co-Processor operation instructions with suitable example. ***(04)***

3C. Discuss the different granularity available in the ARM Memory Management Unit (MMU) architecture. ***(02)***

4A. Write the assembly code and steps to involved in initializing the Instruction Tightly Coupled Memory (TCM) in ARM946E-S. ***(05)***

4B. Describe the condition execution implemented in ARM5VE instruction set with the example. ***(03)***

4C. Explain the significance of sticky flag of CPSR register during saturated arithmetic operation. ***(02)***

5A. Write the different features and application of ARM11 series processor. ***(03)***

5B. Explain the different ARM SIMD instructions specifically used for DSP application. ***(03)***

5C. Sketch the typical AMBA based system, draw the timing diagram for read, and write transfer. ***(04)***