Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, NOVEMBER 2019

FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 26 November 2019** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. For each of the system constraints given below, choose the most appropriate technology among FPGA, standard cell, and full-custom IC technologies for implementing a given circuit. Justify your answers.

i. A system must exist as a physical prototype by next week
ii. The system should be as small and low-power as possible. Short design time and low cost are not priorities.
iii. The system should be reprogrammable even after the final product has been produced.
iv. The system should be as fast as possible and should consume as little power as possible, subject to being completely implemented in just a few months.
v. Only five copies of the system will be produced and we have no more than Rs 1 lakh to spend on all ICs. ***(05)***

1B. Sketch & explain the CMOS based logic circuit for the problem statement given below. A house energy monitor system should sound an alarm if it is night and light is detected inside a room but motion is not detected. ***(03)***

1C. What are the important features and advantages of dynamically reconfigurable FPGAs? ***(02)***

2A. Explain the structure of CLB in Xilinx Spartan IIE highlighting its modes of usage. ***(05)***

2B. For the circuit shown in Fig Q2B give the set of test vectors that detect only all stuck-at-0 faults in the circuit. Make sure to use the minimum number of vectors.

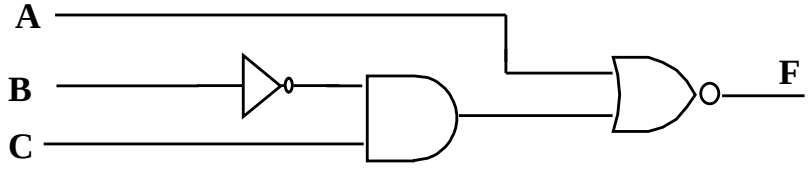

Fig Q2B

(03)

2C. With the help of circuit diagram explain a typical boundary scan cell. ***(02)***

3A. Explain the programming technology used by Actel in FPGAs with necessary diagram. ***(03)***

3B. Write Verilog test bench code for half adder. Display the message "error" if half adder outputs is not matching with expected functionality. Assume the Verilog code for the design under test is available with necessary input and output. ***(03)***

3C. Implement the following digital components using ACT-1 logic module.

i) 4:1 mux ii) 3 input EXOR gate ***(04)***

4A. What are the benefits of using a soft embedded processor in an FPGA over a hard macro implementation? ***(02)***

4B. Draw the synthesized circuit for the Verilog code given.

```
module addborcb(x, a, b, c, d);
input wire [15:0] a, b, c;
 input wire d;
output reg [15:0] x;
reg [15:0] t;
always @ ( a or b or c or d )
begin
 if ( d ) t = b;
else t = c;
 if ( a < 8 )
t = t + 12;
 x = a + t;
end endmodule
```

(04)

4C. Implement digital circuit to add two 3 bit number in Spartan 2E FPGA using

i. LUTs and dedicated mux (if necessary)
ii. LUTs and carry control logic

How many CLBs are required for the implementation? ***(04)***

5A. Which of the following implementations are not possible?

i. A custom processor on an FPGA
ii. A custom processor on a full-custom IC
iii. A programmable processor on an FPGA
iv. A programmable processor on an ASIC
v. A programmable processor on a full-custom IC

Explain your answer. ***(05)***

5B. The impulse response of a linear phase FIR filter is h(n)=[2 1 1 2]. Develop look-up and serial adder based architecture for 4 tap symmetrical FIR filter suitable to implement in an FPGA. Explain the developed architecture. Determine response of developed filter for the input x(n)=[2 1 2]. Mention the partial output for each bit shift of the shift register. ***(05)***