Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
JANUARY 2020
SUBJECT: ANALOG MIXED SIGNAL DESIGN (ECE - 4013)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. i. Compare the performance of basic and cascode current mirror circuits.
ii. State why long channel devices are used in analog design?
iii. Define and explain the significance of following parameters with respect to MOS device: [a] γ [b] η L_{eff}

1B. Give OTA-C implementation of:
i. Floating resistor (series element)
ii. Floating resistor (shunt element)

1C. Explain how the differential operation can reduce following:
i. Effect of supply noise
ii. Effect of coupled noise from digital clock signal.

(4+3+3)

2A. Give the circuit diagram of passive RLC band-pass biquad and then realise voltage mode OTA-C equivalent circuit. Derive the expression for transfer function for both circuits. Give the expression for pole frequency and pole-Q. Obtain expression for single parameter sensitivity as applicable.

2B. Show that integrators can be used to realize second-order oscillators. Discuss two op-amp based oscillator circuit using Deboo integrator. Derive the expression for frequency of oscillation.

2C. Define the following terms: [i] Total harmonic distortion (THD) [ii] Sensitivity

(4+3+3)

3A. Give the fully differential realization of OTA-C biquad based on RLC parallel resonator circuit shown in **Fig. Q3A**. Find the transfer function. Check whether you can also realize a low-pass biquad?

3B. Analyze the circuit given in **Fig. Q3B**. Give your comments. Give the fully differential implementation of the same.

3C. Give the op-amp based circuit for grounded negative resistance and negative capacitance simulation.

(4+3+3)

4A. i. Calculate the small-signal voltage gain A_v for NMOS (M_1) CS stage with diode-connected PMOS load (M_2). Given that $(W/L)_1=50/0.5$, $(W/L)_2=10/0.5$, $\mu_n=2.5\mu_p$ and $I_{ds1}=I_{ds2}=0.5$mA. Assume $\lambda=0$.

ii. With a schematic circuit, explain the working of basic operational transconductance amplifier circuit.

4B. Explain the working of 4-bit current-mode R-2R Ladder DAC. Give the salient features of the same.

4C. Give an account of nonlinearity errors associated with DACs.

(4+3+3)

5A. i. Discuss the Layout considerations for the capacitor array used in charge scaling DAC.

ii. Show how Miller's theorem can be used to realize negative capacitance circuit using OTA.

5B. Discuss OTA-C simulation of parallel LC resonator as a series impedance element.

5C. Explain the following analog layout techniques [i] interdigitization [ii] symmetry

(4+3+3)

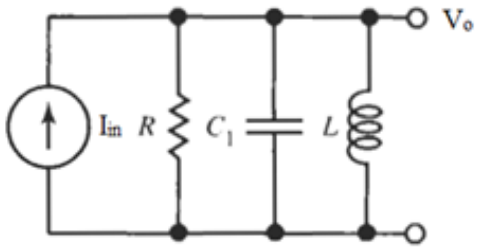

Fig. Q3A

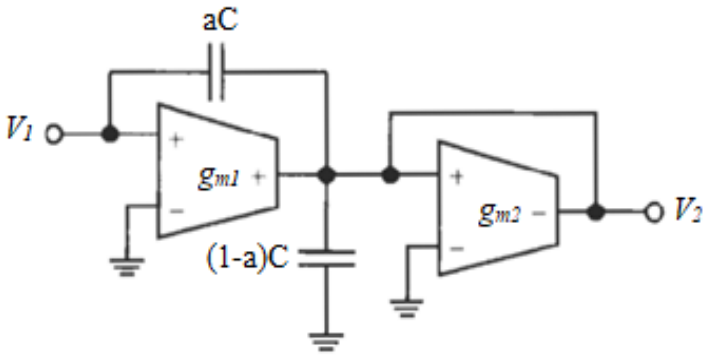

Fig. Q3B