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MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, DECEMBER 2020

FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 26 December 2020** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. What are the important features and advantages of dynamically reconfigurable FPGAs? ***(02)***

1B. Design a digital circuit whose output is an enabling signal for a pushbutton ignition system in automobile. When the output of this circuit is high, the starter is enabled, and pushing the start button will start the car. The start enable output signal should be high (s=1) when all of the three conditions are true.

i. the engine is not already running,
ii. the clutch is depressed,
iii. the emergency brake is ON or the foot brake is depressed

Assume that inputs come from sensors that detect the state of the engine, the clutch and the brakes. Clearly mention when sensor outputs are low and when they are high. Sensor outputs are inputs to the digital circuit.

Implement the circuit using only 2 input LUTs. Give the contents (bits) of all the LUTs. ***(04)***

1C. For the circuit in Fig Q1C give the set of test vectors that detect only all stuck-at-0 and stuck-at-1 faults in the circuit. Make sure to use the minimum number of vectors. Clearly indicate the faults detected for each test vector. ***(04)***

2A. A home security system has 8 sensors that detect open doors and windows. Each sensor produces a digital 0 when the window or door is closed and 1 when the window or door is open. The control for the security system repeatedly checks each of the 8 sensors. The digital system repeatedly checks the digital signal at the 8 sensors and display the sensor number and corresponding digital signal. Sensors are numbered as 0 to 7. Draw the system level block diagram description mentioning necessary digital components for the given security system. ***(02)***

2B. Design a digital system to control an automatic sliding door with the following conditions. An input 'p' to the digital system indicates whether a sensor detects a person in front of the door. An input 'q' indicates whether the door should be manually held open regardless of whether a person is detected. An input 'r' indicates whether the door should be forced to stay closed. r=1 means the door should stay closed. Implement the digital circuit using Actel ACT-1 module. ***(03)***

2C. Sketch the basic block diagram of Xilinx Spartan IIE FPGA and briefly explain the major configurable elements. ***(05)***

3A. Draw the state diagram for the serial adder shown in Fig. Q3A. Inputs to the state machine are x_i and y_i. Output is sum_i. ***(03)***

3B. A logic circuit library shown in Fig Q3B(a) has collection of OR, AND gates with some delay and power specifications. Optimize the digital circuit shown in Fig 3QB(b) by reducing the power consumption without increasing the circuit's delay. Refer to the logic circuit library for the options available. ***(03)***

3C. Given the circuit (Fig Q3C(a)) and the configurable logic block (CLB) (Fig Q3C(b)), partition the circuit so that it can be implemented with a collection of CLBs. Try to use as few a number of CLBs as possible. Indicate your answer by filling in the table: one row per CLB used; for the configuration bit, s, write in a '0' or '1', for all other columns write in the name of the signal wire from the logic circuit that corresponds to the CLB input or output, a '0' or '1', or nc for no connection. You may leave some rows blank or add rows.

CLB #	u	v	w	x	y	z	s
1							
2							
3							
4							
5							
6							
7							
8							

(04)

4A. Draw the circuit for the transmission gate based 2 input LUT. Explain the circuit. ***(02)***

4B. Design an LFSR (linear feedback shift register) with n=4 that generates a maximum length random sequence. Modify the circuit to include 0000 in the generated sequence. Mention the sequence in both cases. ***(03)***

4C. The impulse response of a linear phase FIR filter is h(n)=[2 1]. Develop FPGA based architecture for two bit parallel distributed arithmetic FIR filter. Explain the developed architecture. Determine response of developed filter for the input x(n)=[5 3]. Mention the partial output for each bit shift of the shift register. ***(05)***

5A. What are the functions of test access port pins? What is the need for this architecture? ***(02)***

5B. Explain the partial reconfigurable design flow with diagram and chart ***(03)***

5C. A digital sequential circuit with additional architecture for scan path testing is shown in figure Fig Q5C. There is stuck-at-1 fault at position H. Choose one of the appropriate present state and input x and explain how stuck-at-1 fault at position H can be detected through additional scan path test architecture shown in Figure. Draw the timing diagram. Mention about the next state of the finite state machine without stuck-at-1 fault and with stuck-at-1 fault at H. ***(05)***

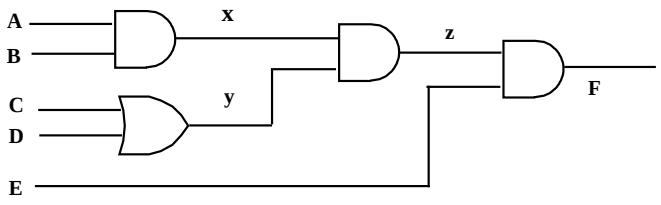

Fig Q1C

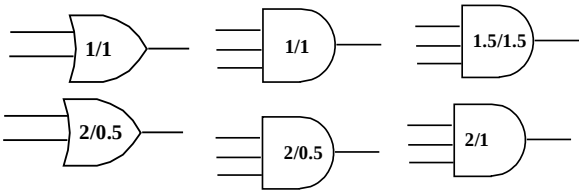

Fig Q3B(a): Logic gate Library: 2/0.5 format means 2 ns delay/0.5 mw power

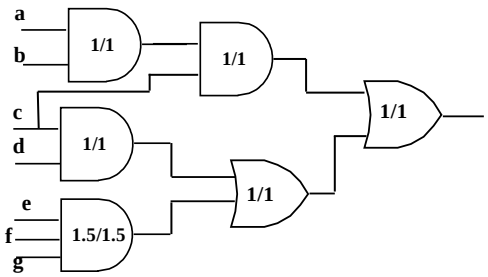

Fig Q3B(b): Digital circuit

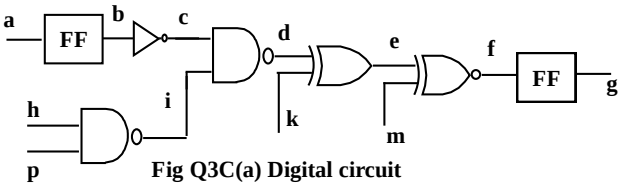

Fig Q3C(a) Digital circuit

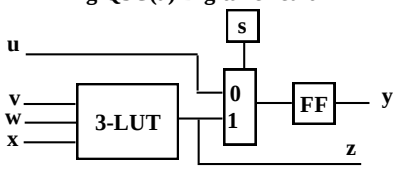

Fig Q3C(b) Configurable Logic Block (CLB)

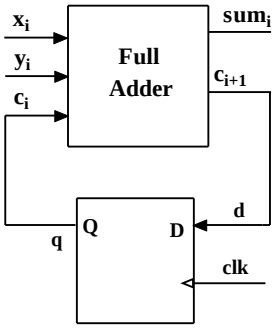

Fig. Q3A

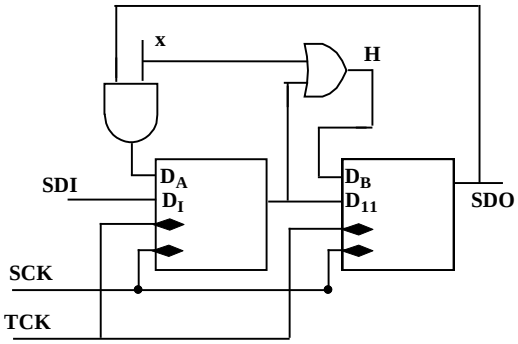

Fig. Q5C