INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL

B.Sc. (Applied Sciences) in Engg.

End – Semester Theory Examinations – Nov./ Dec. 2020

II SEMESTER - COMPUTER ORGANIZATION & ARCHITECTURE (ICS 122)

(Branch: CS)

Time: 3 Hours **Date: 07 December 2020** **Max. Marks: 100**

- ✓ **Answer any FIVE full questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. Convert the following pairs of decimal numbers to 2's-complement numbers, then add them and subtract the second number from the first number. Take enough no. of bits to avoid overflow.

i) -15 and -10
ii) +14 and +16
iii) -18 and 12

1B. Use the Booth algorithm to multiply 13 (multiplicand) by 9 (multiplier). Show the intermediate values of the registers

(6M+14M)

2A. Consider a computer that has a byte-addressable memory organized in 32-bit words according to the big-endian scheme. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the word "Computer" has been entered. Repeat the same for the little-endian scheme.(ASCII codes: c-43, o-6F, m-66, p-70, u-75, t-74, e-65, r-72)

2B. Registers R4 and R5 contain the decimal numbers 4000 and 6000 respectively, before each of the following addressing modes is used to access a memory operand. What is the effective address (EA) in each case?

15(R4)
(R4, R5)
30(R4, R5)
(R5)

(10M+10M)

3A. Write the flow chart of Booth's algorithm for signed multiplication and explain. Using this algorithm multiply -4 (multiplicand) by +10 (multiplier). Write all the steps showing the intermediate values in the registers.

3B. Write and explain the micro operations for interrupt cycle, by making use of data flow diagram and sequence of events.

(10M + 10M)

4A. Draw the block diagram of a computer with its essential components, showing the connection between processor and memory. List the steps needed to execute the instruction

Load R2, LOC

4B. What do you mean by normalized floating point number? How it is used in 32-bit floating point representation? Represent +25.625 in 32-bit floating point format.

(10M+10M)

5A. Compare CISC with RISC instruction sets

5B. Explain two stage machine algorithm for dynamic branch prediction.

The two states are:

LT - Branch is likely to be taken

LNT - Branch is likely not to be taken

(8M+12M)

6A. Draw the block diagram of hardware for addition and subtraction of integers and explain its operation

6B. Explain the following with respect to memory systems.

i) Memory access time
ii) Memory cycle time
iii) EEPROM
iv) Virtual memory

(8M+12M)

7A computer has a memory of 64K words and a cache of 1K words with a block size of 4 words. Determine the number of bits in the main memory address and the cache memory address. Show the main memory address format if the mapping technique used is

i) Direct mapping
ii) 4 way set associative mapping.

7B. Explain UMA and NUMA multiprocessor systems**.** **(8M+12M)**

8A. With necessary diagram explain how a virtual address is translated to a physical address. Consider the virtual address space specified by 20 bits. The byte addressable main memory size is 64 kilobytes. If the page number field of the virtual address is 9 bits, find the following:

i) Size of the virtual memory
ii) Number of bits needed to specify the main memory address
iii) Number of pages
iv) Size of a page
v) Number of blocks in the main memory.

8B. What is instruction hazard? Explain with respect to unconditional branching.

(12M+8M)

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