INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL
B.Sc. (Applied Sciences) in Engg.
End – Semester Theory Examinations – Nov./ Dec. 2020
III SEMESTER - ANALOG ELECTRONIC CIRCUITS (IEC 231)
(Branch: CS)

Time: 3 Hours **Date: 19 November 2020** **Max. Marks: 100**

- ✓ **Answer Any Five Full questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. Draw the circuit diagram of common emitter configuration using NPN transistor. Draw and explain the input and output characteristics. Indicate cut-off, saturation and active regions. 10M

1B. The CS stage shown in **FIG 1B** must achieve a voltage gain A_V = 15 at a bias current of 0.5mA. If $\lambda_1 = {}^{0.15}/_{V}$ *and* $\lambda_2 = {}^{0.05}/_{V}$, determine the required value of $\left({}^{W}/_{L}\right)_2$. Assume $\mu_P C_{OX} = 100\,\frac{\mu A}{V^2}$

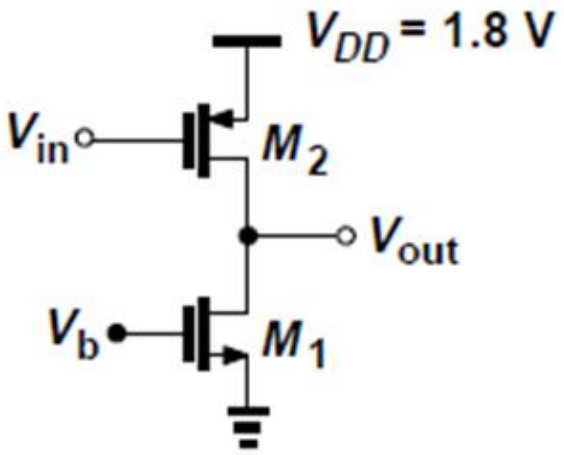

Fig 1B 10M

2A. Draw the circuit diagram of a common source stage using NMOSFET, with drain resistance R_D. Draw the small signal model of the circuit. Obtain the expression for the voltage gain and output resistance. Assume $\lambda \neq 0$. 10M

2B. Determine I_B, I_C, I_E, V_{CE}, V_B, V_C and V_E for the voltage divider configuration shown in **Fig 2B** given that β=80. Assume V_{BE}=0.7V. What is the region of operation? Neglect I_{CO}.

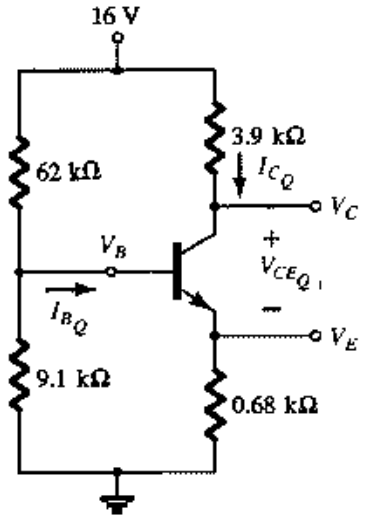

Fig 2B 10M

3A. Draw the circuit diagram of a common source stage using a NMOSFET, with NMOS diode connected as load. Draw the small signal model of the circuit. Obtain the expression for the voltage gain and output resistance. Assume λ≠ 0. 10M

3B. State and explain Millers theorem with an illustration. Explain any one application of this theorem with necessary circuit 10M

4A. Draw the circuit diagram of RC coupled amplifier with feedback using NPN transistor. Mention the function of each component. Explain the working at low, medium and high frequencies. 10M

4B. The degenerative CS stage of **Fig. 4B** must provide a voltage gain of 4 with a bias current of 1 mA. Assume a drop of 200 mV across R_S and λ=0. If R_D =1KΩ, determine the required value of W/L. Does the transistor operate in Saturation for this choice of W/L? Assume $\mu_n C_{OX} = 200\frac{\mu A}{V^2}, V_{th} = 0.4V$.

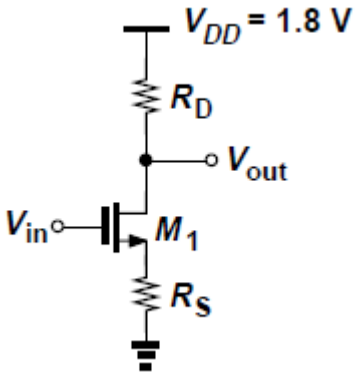

Fig. 4B 10M

5A. Draw the circuit diagram of a crystal oscillator and explain the working. Mention any two advantages of Crystal oscillators. 10M

5B. Draw the circuit diagram of a common source stage using a NMOSFET, with a source degeneration resistance R_S. Draw the small signal model of the circuit. Obtain the expression for the voltage gain (Assume $\lambda=0$) and output resistance with the assumption $\lambda \neq 0$. 10M

6A. Draw the circuit diagram of a common source stage using NMOSFET, with a PMOS current source. Draw the small signal model of the circuit. Obtain the expression for the voltage gain and output resistance. Assume $\lambda \neq 0$. 10M

6B. With the help of a circuit diagram, explain the working of transformer coupled Class B push pull power amplifier. Derive an expression for the maximum power efficiency. Mention one drawback of this amplifier. 10M

7A. Draw the block schematic of i) Voltage shunt ii) Current series feedback amplifiers. What is the effect of series and shunt feedback on the input and output resistance of an amplifier? 10M

7B. For the transistor (Silicon) circuit shown in F**ig.7B**, $R_{in} = 100K\Omega, R_L = 820\Omega$ and $V_{CC} = 10V$. Assume $V_{BE,\ sat}$=0.8V and V_{CE}sat = 0.2V. Find the minimum base and collector current required in order to keep the transistor in saturation. Neglect $I_{CBO.}$ Explain briefly the working of the circuit and draw the output waveform.

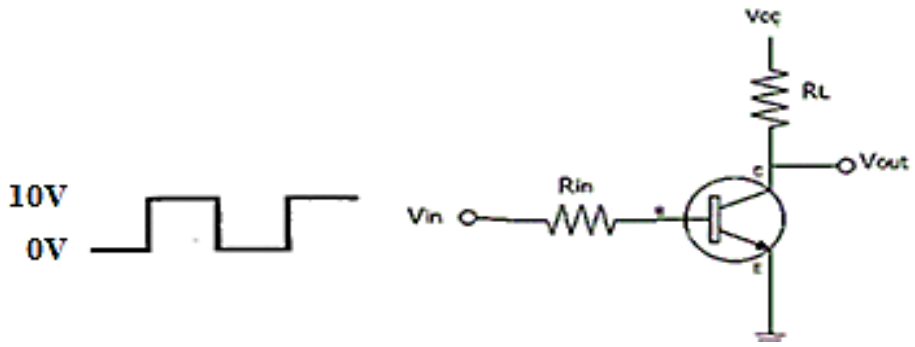

Fig. 7B 10M

8 Explain the following: 4x5=20M

i) Early effect in BJT
ii) Channel length modulation in MOSFET
iii) Advantages and disadvantages of Positive and Negative feedback.
iv) Piezoelectric effect in crystals.

****