Reg. No. | | | | | | | | | | |

# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*(A constituent unit of MAHE, Manipal)*

**SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)**

**END SEMESTER DEGREE EXAMINATIONS, DECEMBER - 2020**

**SUBJECT: VLSI DESIGN [ICE - 4004]**

**01-01-2021**

TIME: 3 HOURS MAX. MARKS: 50

**Instructions to candidates :*Answer ALL questions and missing data may be suitably assumed.***

1A. Illustrate Moore's first law.

1B. What is Pinch-off phenomenon? Explain.

1C. Explain the n-well fabrication process.

(2+3+5)

2A. What are the objectives of BIST? How are they achieved?

2B. Explain the working of an nMOS inverter.

2C. What are the building blocks of FPGA? Differentiate between FPGAs and ASICS.

(2+3+5)

3A. What are the advantages of using lambda based designs?

3B. Explain latch-up in p-well structures.

3C. What are the different regions of operation of a CMOS inverter? Explain with a diagram and relevant equations.

(2+3+5)

4A. Derive the sheet resistance Rs for a conducting material of resistivity ρ, width w, thickness t and length between faces L.

4B Obtain the scaling factors for gate capacitance per unit area, gate capacitance and parasitic capacitance.

4C Draw a 2 Input NOR gate in CMOS logic and represent it using stick notation.

(2+3+5)

5A. What are the guidelines to be followed while tackling large transistor designs?

5B. Design a parity generator in CMOS logic.

5C. With neat diagrams, explain the process of scan path testing.

(2+3+5)

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