Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIRST/SECOND SEMESTER B.TECH DEGREE END SEMESTER EXAMINATION

AUGUST 2021

SUBJECT: BASIC ELECTRONICS(ECE-1051)

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates

- Answer **ANY FOUR FULL** questions.
- Missing data may be suitably assumed.

1A. Consider a bridge rectifier with four identical Silicon diodes. If the primary voltage is 120V, 60Hz, turns ratio is 5:1 and the load resistance is 1KΩ, Find the average and rms value of load voltage, efficiency, ripple factor, PIV rating and frequency of the output waveform

1B. Draw the circuit of Zener regulator and explain the principle of load and line regulation. Consider a Zener regulator that regulates at 50V over a range of diode current 5 mA to 40 mA. If the supply voltage is 200V, calculate the value of series resistance 'R_s' to allow voltage regulation for load current variation I_L = 0 to Imax.

(5+5)

2A. Sketch the input and output characteristics of NPN transistor in CB Configuration indicating various regions of operation. Consider a fixed bias circuit using Silicon transistor with V_{CC} =10V, R_C=500Ω and R_B = 100KΩ. Find and mark the Operating point on the output characteristics. Assume β=100.

2B. Draw the circuit of RC Coupled amplifier and explain the role of each component. Sketch its frequency response indicating cutoff frequencies and bandwidth. In a three-stage amplifier, the voltage gain of first stage is 40 dB, gain of second stage is 200 (not in dB) and that of third stage is 0 dB. Find the overall gain of the amplifier

(5+5)

3A. Draw the circuit of OP-AMP inverting adder and derive an expression for output voltage for three input voltages. Also, Realize the equation $V_0 = 3V_1 - 0.8V_2 + 0.5V_3$ using two OP-AMPS.

3B. Draw the circuit of OP-AMP Comparator and explain the working principle. A step input signal of V_i=1V is applied to an OP-AMP integrator with R_1=10 KΩ and C_f=10nF. Find the output voltage at t=0.3ms & plot the output waveform for the time interval 0 to 0.3ms.

(5+5)

4A. In a certain application, four inputs A, B, C, D are fed to a logic circuit, producing an output Z which controls a relay. Z = 1 for the input states (ABCD): 0000, 0010, 0101, 0110, 1101 and 1110. The states 1000 and 1001 do not occur and Z = 0 for the remaining input states.

i. Obtain truth table for Z.
ii. Use Karnaugh map to find a minimal SOP and implement the same using NAND gates only.

4B. Draw the logic circuit of 3 bit up counter using negative edge triggered JK flip-flops. Also sketch the timing diagram.

(5+5)

5A. Differentiate between sequential & combinational circuits. Consider a serial input data 11100110 fed to a 4-bit shift register circuit from LSB. What will be the output for SISO operation after 6th clock pulse? How many clock pulses are required to shift MSB bit to the output? Also, draw the circuit diagram.

5B. With necessary illustration, define FM. A frequency modulated voltage is given by, $e=12\sin(10^7t+2sin10^3t)$. Calculate the carrier frequency, modulating frequency, modulation index and frequency deviation.

(5+5)

6A. Define amplitude modulation. Sketch the spectrum of AM signal indicating sideband frequencies, amplitudes and bandwidth. A certain AM transmitter radiates 9 kW of power with carrier unmodulated and 10.125kW of power when carrier is sinusoidally modulated. Calculate the modulation index.

6B. Draw the block diagram of digital communication system and highlight the function of each block. Also, Sketch ASK and FSK signals for the binary data 10010.

(5+5)