Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

III SEM B.Tech (BME) DEGREE END SEMESTER EXAMINATIONS, MARCH 2021

SUBJECT: DIGITAL ELECTRONICS (BME 2153)
(REVISED CREDIT SYSTEM)
Friday, 5th March, 2021: 9 AM to 12 NON

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer ALL questions.**
2. **Draw labeled diagrams wherever necessary.**

1A. Depicting the necessary steps and calculations perform the following: 04

(a)*Subtract the following BCD numbers using* $1's$ *complement method*

(i) 45 *from* 71 (ii) 95 *from* 62

(b) *Convert into,*

$(i)\ (65.25)_{10} = (\quad)_2$ $(ii)\ (364.32)_8 = (\quad)_{10}$

1B. Simplify the following functions to a minimum number of literals using Boolean simplifications. 03

$(i)\ F(ABC) = (A+B) + \overline{[\bar{A}(\bar{B}+\bar{C})]} + \bar{A}\bar{B} + \bar{A}\bar{C}$

$(ii) F(ABC) = [A\bar{B}(C+BD) + \bar{A}\bar{B}]C$

$(iii)\ f(xyz) = \overline{[\bar{x}\,(\,\bar{y}+\bar{z})(x+y+\bar{z}\,)]}$

1C. Realize a half adder and draw the circuit using (i) Basic Gates. (ii) Minimum numbers of two input NAND gates. 03

2A. Design and draw the circuit of 1 digit BCD adder using IC 7483 and with additional gates. Explain its operation with suitable examples considering all three conditions. 04

2B Simplify the following function using Karnaugh map and realize and draw the circuit using only NAND gates. 03

$$F(ABCD) = \sum 0,3,4,5,7,8,9,13,15$$

2C. Realize and draw the circuit of 2×4 line decoder using appropriate gates with active low outputs and active low Enable line. How this circuit can be used as 1×4 line De-multiplexer? 03

3A. Design and draw the decoder circuit to convert BCD code into Gray code. 04
Consider $F(ABCD) = \sum(10, 11,12,13,14,15)$ are don't care combinations.

3B. Realize and draw the circuit of Octal to Binary Encoder using diode matrix. 03

3C. Realize the following function using 4×1 Multiplexer with A and B are the select lines and C and D are the input lines. 03

$$F(A,B,C,D) = \sum 0,1,3,5,6,7,8,9,11,12,15$$

4A. Realize and draw the complete circuit of a ROM using diode matrix to realize the following truth table. Also mention the memory size of the ROM. 04

INPUTS				OUTPUTS			
A	B	C	D	W	X	Y	Z
0	0	1	0	1	0	0	1
0	1	1	0	1	1	0	0
1	0	1	0	0	0	1	1
1	1	0	1	1	1	1	0

4B. Draw the circuit of a D flip flop using NAND gates. Explain the operation of the circuit with suitable truth table. Also write the excitation table of this flip flop. 03

4C Draw the circuit of MOD-13 asynchronous counter using JK- flip flops. Write the count sequence and draw the timing waveforms. 03

5A. Design a synchronous counter to count the following count sequence using JK flip flops. Also verify the counting with timing waveforms. 04

$000, 001, 010, 011, 100, 101, 110, 000, \ldots \ldots$

5B. Draw the circuit of a 3 bit shift register using D flip flops to operate as (i) PIPO (ii) PISO. Explain the operation with the appropriate truth table. 03

5C. Draw the circuit of a Mod-8 Johnson counter. List the legal and illegal count sequences. Give a remedy circuit to avoid the illegal counts. Also draw the necessary decoder circuit to read the legal counts. 03