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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*(A constituent unit of MAHE, Manipal)*

## III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

## GRADE IMPROVEMENT/MAKEUP EXAMINATIONS, JULY 2021

SUBJECT: DIGITAL SYSTEM DESIGN [CSE 2153]

**REVISED CREDIT SYSTEM**
**(23/07/2021)**

Time: 2 Hours MAX. MARKS: 40

**Instructions to Candidates:**

- Answer **FOUR** full questions.
- Missing data may be suitably assumed.

**1A.** Obtain the minimum cost SOP and POS for the following function F using K-map. F(a, b, c, d, e) = πM (0, 2, 6, 10, 13, 14, 18, 25, 26, 30). **5M**

**1B.** Use functional decomposition to find the best implementation of the function f(a,b,c,d,e )= Σm(1, 2, 5, 7, 9, 10, 13, 15, 18, 19, 25, 26, 29, 31). **5M**

**2A.** Design a circuit which generates the magnitude of a 5-bit signed number A[4:0] in binary using half adders, multiplexers and NOT gates. Explain the working of your design. **6M**

**2B** Use Shannon's Expansion to implement f(a,b,c,d,e)=bd' + cd + a'c taking a,b,c as select lines. Use 8:1 multiplexer and other necessary gates. **4M**

**3A.** Write the truth table for a 4 input XOR function. Implement it using least possible number of 4:1, 2:1 multiplexers and NOT gates. **5M**

**3B.** A 2:4 priority encoder is designed as shown in the Table P.15. Based on the table answer the following questions:

a) Which variable has the highest priority?
b) Which variable has the lowest priority?
c) What is the output y and z for input "0101"?
d) What is the output y and z for input "0011"?

**5M**

Table P.15.

| w3 | w2 | w1 | w0 | y1 | y0 | z |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | d | d | 0 |
| 0 | 0 | 1 | x | 0 | 0 | 1 |
| 0 | 1 | x | x | 0 | 1 | 1 |
| 1 | x | x | x | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**4A.** A MN Flip Flop (FF) has 2 inputs M and N which are equivalent to the J and K inputs of JK FF respectively. The output of MN FF is the complement of JK FF output.

a. Tabulate the characteristic table of the FF
b. Tabulate the excitation table of the FF
c. Derive the characteristic equation for Q(t+1) in terms of Q(t), M and N.
d. Using MN FF design a Mod 8 binary down counter. **4M**

**4B.** Design a counter with the repeated binary sequence 1, 3, 5, 7, 2, 4, 8, 10, 12, 14 using SR Flip Flops. Treat unused states as don't cares. Write the Flip Flop input equations **6M**

**5A.** Define Programmable Logic Devices(PLDs). State four differences between the two different types of PLDs. Draw the customary schematic for the PLD which implements the two functions given below using programmable AND and OR gates.

$F(a,b,c) = \sum m(0,2,3,7)$
$G(a,b,c) = \prod M(0,1,4,6)$ **5M**

**5B.** Derive the state diagram for an FSM that has an input *w* and an output *z*. The machine has to generate $z=1$ when the previous four values of *w* were 1001 or 1111; otherwise $z=0$. An example of the desired behaviour is

| w | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| z | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

Derive the next-state and output equations for the obtained FSM. **5M**

**6A** Draw the state diagram and ASM chart for a control circuit that swaps the contents of registers R1 and R2, in response to an input w = 1. Indicate the control signals in each state in the state diagram. **5M**

**6B** With a neat diagram explain how data transfer between the registers takes place in a computer system **5M**